Available online at www.bpasjournals.com

Reliability and Power Loss Investigation of Hybrid Multilevel Inverter for Symmetrical/Asymmetrical Sources with Optimized Power Conversion

Prateek Nigam^{1*}, Ashish Jain², Kishor Thakre³

¹PhD Scholar, Department of Electrical & Electronics Engineering, Shri Shankaracharya Technical campus, Bhilai (C.G.), INDIA, prithagupta.25@gmail.com

How to cite this article: Prateek Nigam, Ashish Jain, Kishor Thakre (2024) Reliability and Power Loss Investigation of Hybrid Multilevel Inverter for Symmetrical/Asymmetrical Sources with Optimized Power Conversion. *Library Progress International*, 44(3), 8190-8198.

ABSTRACT

Hybrid multilevel inverters (MLIs) for symmetrical and asymmetrical sources have become a vital technology for modern power conversion systems, particularly in renewable energy and industrial applications. This paper investigates the reliability and power loss characteristics of hybrid MLIs, focusing on the combination of symmetrical and asymmetrical DC sources for enhanced power efficiency. Through analytical modeling, simulation, and prototype setup the paper highlights power losses and system reliability of proposed hybrid multilevel inverter on the basis of the design parameters. Practical solutions are also proposed for minimizing power loss and maximizing reliability, making hybrid MLIs an effective solution for sustainable and high-performance energy conversion systems.

Keywords: H Bridge Hybrid multilevel inverter (HBHMLI); symmetrical sources; asymmetrical sources; reliability, power loss, energy efficiency; optimized power conversion; renewable energy.

1. Introduction

The increasing demand for reliable and efficient power conversion systems, driven by the rise in renewable energy technologies and industrial automation, has led to the development of hybrid multilevel inverters (MLIs). These inverters, by utilizing multiple voltage levels, offer numerous benefits such as reduced harmonic distortion, higher power quality, and lower electromagnetic interference (EMI) [1]. Hybrid MLIs, which combine both symmetrical and asymmetrical sources, provide greater design flexibility and efficiency compared to traditional MLI architectures. The objective of this research is to investigate the reliability and power loss mechanisms in hybrid MLIs, particularly focusing on the integration of symmetrical and asymmetrical sources. This paper analyzes the various factors affecting power loss and reliability and presents strategies for optimizing the inverter's performance. The results provide valuable insights for researchers seeking to develop advanced MLIs with

² Associate Professor, Department of Electrical & Electronics Engineering, Shri Shankaracharya Technical campus, Bhilai (C.G.), INDIA, singhs004@gmail.com

³Professor, Department of Electrical & Electronics Engineering, Shri Shankaracharya Technical campus, Bhilai (C.G.), INDIA, shimpy.ralhan@sstc.ac.in

⁴Department of Electrical Engineering, Bhilai Institute of Technology, Durg (C.G.), INDIA, sp.shukla@bitdurg.ac.in,

⁵Department of Electrical Engineering, Bhilai Institute of Technology, Durg (C.G.), INDIA, supriya.tripathi@bitdurg.ac.in

enhanced energy efficiency and system robustness. PSIM software is widely used for simulating power electronics systems due to its user-friendly interface and robust simulation capabilities.

For the symmetrical configuration, identical DC voltage sources are connected to each H-bridge cell. In the asymmetrical configuration, different DC voltage sources are used, typically in a binary sequence to maximize the number of output levels [2]. The simulation setup for the HBHMLI topology involves designing the inverter circuit, setting up the control strategy, and analyzing the performance under different source configurations. The circuit design in PSIM involves creating the H-bridge inverter cells and integrating the auxiliary circuits. Each H-bridge cell consists of four IGBTs configured to generate three voltage levels (positive, negative, and zero). The auxiliary circuits, composed of diodes and additional IGBTs, are connected to the H-bridge cells to achieve the desired seven-level output. The prototype experimental setup is also design inn the breadboard to validate the reliability operation.

2. H Bridge Hybrid Multilevel Inverter Architecture

Multilevel inverters (MLIs) are designed to produce high-quality sinusoidal waveforms by synthesizing multiple voltage levels. This is achieved using a combination of power switches, capacitors, and DC sources, which can either be symmetrical (equal voltage sources) or asymmetrical (unequal voltage sources). The simulation of the h bridge hybrid multilevel inverter is presented in figure 1.1

Key advantages of MLIs include:

- Reduced total harmonic distortion (THD): Higher voltage levels improve the quality of the output waveform.
- Lower switching losses: Operating at lower switching frequencies reduces the stress on power devices.
- **High efficiency**: MLIs can achieve high conversion efficiencies, making them ideal for grid-connected renewable energy systems.

2.2 Symmetrical and Asymmetrical Source Configurations

- Symmetrical Source MLI: Uses equal DC voltage sources across multiple stages to produce a fixed number of voltage levels. This configuration is simpler to implement but may require more components to achieve higher voltage levels.
- **Asymmetrical Source MLI**: Uses unequal DC voltage sources, allowing for more voltage levels with fewer components. This increases the inverter's flexibility but adds complexity to the control algorithm.

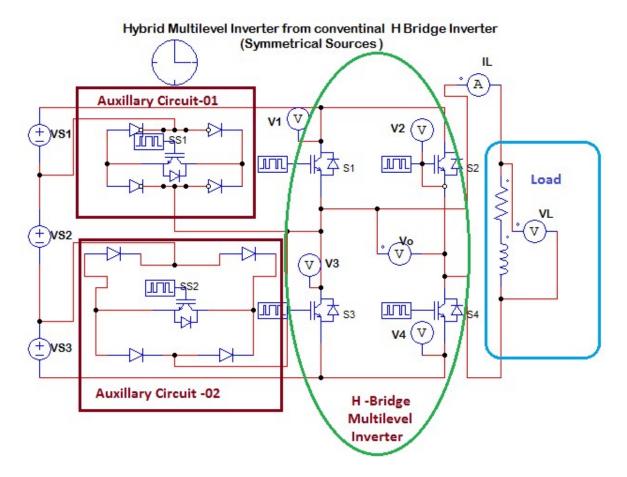


Figure-1.1: Proposed H Bridge Hybrid Multilevel inverter

3. Switching Topology and Modes of operation

The HBHMLI employs a sophisticated switching topology to achieve seven distinct voltage levels: ± 300 V, ± 200 V, ± 100 V, and 0V. This is accomplished through specific conduction states of the main H-bridge switches (S1, S2, S3, S4) and the auxiliary switches (SS1, SS2), as detailed in the table.

- In Mode-01, to produce a voltage level of 300V, switches S1 and S4 are turned on (S1=1, S4=1) while SS1 and SS2 are off (SS1=0, SS2=0).
- In Mode-02, a voltage of 200V is achieved by turning on S4 and SS1 (S4=1, SS1=1), with S1, S2, S3, and SS2 all off (S1=0, S2=0, S3=0, SS2=0).
- Mode-03 generates 100V by having S4 and SS2 on (S4=1, SS2=1), while S1, S2, S3, and SS1 remain off (S1=0, S2=0, S3=0, SS1=0).
- For Mode-04, to produce 0V, switches S3 and S4 are on (S3=1, S4=1), with all other switches off (S1=0, S2=0, SS1=0, SS2=0).

For the negative voltage levels,

• Mode-05 creates -100V by turning on S2 and SS1 (S2=1, SS1=1), while S1, S3, S4, and SS2 are off (S1=0, S3=0, S4=0, SS2=0).

- Mode-06 generates -200V with S2 and SS2 on (S2=1, SS2=1) and the rest of the switches off (S1=0, S3=0, S4=0, SS1=0).
- Lastly, in Mode-07, the -300V level is achieved by turning on S2 and S3 (S2=1, S3=1) with all other switches off (S1=0, S4=0, SS1=0, SS2=0).

This intricate switching topology allows the HBHMLI to precisely control the output voltage levels, enhancing the waveform quality and reducing harmonic distortion [3]. By carefully managing the conduction states of both the main and auxiliary switches, the inverter achieves high performance and efficiency in both symmetrical and asymmetrical configurations. Table 3.1 presents the switching states of the proposed HBMI.

Modes Voltage **Conduction States** Levels (V) S1 S2 S4 SS1 SS2 S3 Mode-01 Mode-02 Mode-03 Mode-04 Mode-5 -100 Mode-06 -200 -300 Mode-07

Table-3.1 Switching Topology

4. Hardware Implementation of H Bridge Hybrid Multilevel Inverter

The hybrid MLI combines both symmetrical and asymmetrical voltage sources in a single topology to maximize the benefits of both configurations. This design reduces the number of components required while still offering high-quality output waveforms with reduced switching losses [4,5].

In hardware prototype shown in fig.4.1 a supply voltage of 230V is steeped down to 12 V and 24 V and 48 V using a step down transformer, which is then transformed to Direct Current using a diode bridge rectifier. The rectified voltage is then fed to the hybrid multilevel inverter inputs circuit as an asymmetrical source. The required components for hardware setup are shown in table4.1.

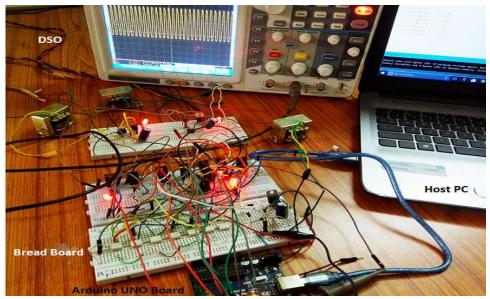


Fig.4.1. Hardware Prototype for H bridge hybrid multilevel inverter Table.4.1 Component used for hardware Setup

S.N0	Name of Component	Specification
1	MOSFET	IRF630fp
2	Step down transformer	0-12V, 5mA;0-24V, 5mA
3	Diode	IN4007
4	Capacitors	1000μF
5	Bridge Rectifier IC	DB105
6	Opto coupler	MCT2E
7	Resistors	1kΩ
8	Voltage Regulator IC	7812, 7824
9	Arduino UNO	 ATmega328 microcontroller Input voltage - 7-12V 14 Digital I/O Pins (6 PWM outputs) 6 Analog Inputs 32k Flash Memory 16Mhz Clock Speed
10	Led	2.0-2.5V, 50mA

The fundamental motivation behind driver circuit is to improve the switching voltages for the MOSFET and also it gives the isolation between power circuit and the micro controller circuit [6,7]. The output from driver circuit is is given across gate and emitter of the MOSFET. MCT2E opto-coupler is used signal for microcontroller is given to given to driver circuit. The hardware is has been interfaced to the Arduino for giving the PWM pulses to the MOSFET [8,9].

5. Reliability Analysis of Hybrid MLIs

The reliability of hybrid MLIs is a crucial concern, especially in long-term operations such as renewable energy integration and industrial power systems [10]. The hybrid configuration introduces multiple components—power switches, capacitors, inductors, and control circuitry—that are prone to failures due to various factors:

- Thermal stress: High temperatures generated by power devices, such as IGBTs and MOSFETs, can lead to thermal fatigue and eventual failure.
- **Electromagnetic interference (EMI)**: The switching operations generate EMI, which can degrade the performance of control circuits and reduce the overall reliability of the system.
- Component aging: Passive components, such as capacitors and inductors, are subject to wear over time, which impacts the inverter's reliability.

The reliability of hybrid MLIs is influenced by several key factors:

- **Operating conditions**: Inverter reliability can degrade due to irregular input power from renewable sources or fluctuations in load conditions.
- **Power device stress**: The increased number of switches and components in hybrid MLIs can result in higher thermal and electrical stresses, particularly in high-power applications.
- **Control complexity**: The combination of symmetrical and asymmetrical sources increases the complexity of control algorithms, which can affect the long-term stability of the system.

To enhance the reliability of hybrid MLIs, the following strategies are proposed:

- **Redundant configurations**: Introducing redundancy in critical components, such as power switches, can ensure uninterrupted operation in case of component failure.
- Advanced thermal management: Utilizing heat sinks, liquid cooling systems, and advanced semiconductor materials, such as SiC (silicon carbide) and GaN (gallium nitride), can help reduce thermal stress and increase system lifespan.
- **Fault-tolerant control algorithms**: Implementing intelligent fault detection and recovery techniques can help maintain system stability in the event of a component failure.

5.1. Fault Tolerance and Reliability Analysis

Fault tolerance is an essential aspect of multilevel inverters, especially in high-power applications [11,12]. The HBMI topology, with its modular design and auxiliary circuits, offers enhanced fault tolerance and reliability. Voltage stress on the switching devices is a critical factor affecting the reliability and lifespan of the inverter. The simulation results for both configurations show that the HBMI topology effectively distributes the voltage stress across multiple IGBTs, reducing the stress on individual devices.

• Symmetrical Configuration

In the symmetrical configuration, the voltage stress is evenly distributed among the IGBTs, resulting in lower thermal stress and reduced switching losses. The overall efficiency of the HBMI in the symmetrical configuration is around 95-97%, making it suitable for applications where efficiency is a critical factor.

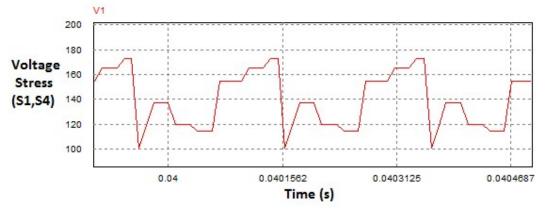


Figure 5.1: Voltage stress across switch S1 and S4 (symmetrical source)

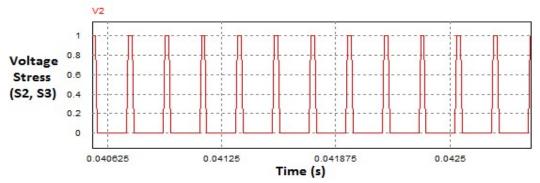


Figure 5.2.: Voltage stress across switch S2 and S3 (symmetrical source)

• Asymmetrical Configuration

The asymmetrical configuration results in higher voltage stress on certain IGBTs due to the different DC voltage levels. However, the use of auxiliary circuits helps in mitigating this stress, ensuring that the overall system reliability is maintained. The efficiency of the HBMI in the asymmetrical configuration is slightly lower, around 93-95%, due to the increased complexity of the control strategy and higher switching losses.

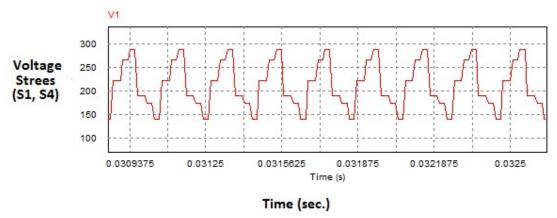


Figure 5.3: Voltage stress across switch S1 and S4 (asymmetrical source)

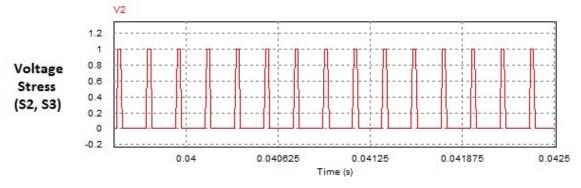


Figure 5.4: Voltage stress across switch S2 and S3 (symmetrical source)

6. Power Loss Mechanisms in Hybrid MLIs

The total power loss in hybrid MLIs primarily comprises conduction losses and switching losses:

- Conduction losses: These occur during the "on" state of the power devices, where current flows through the internal resistance of the devices. Conduction losses depend on the current and the on-state resistance of the switches.
- Switching losses: These losses occur during the transition between the "on" and "off" states of power devices. Switching losses are directly related to the switching frequency, the voltage across the device, and the current through it.

In addition to semiconductor losses, significant power losses can also occur in the passive components of the inverter:

- Capacitor losses: These losses are due to the equivalent series resistance (ESR) of capacitors, which causes heat dissipation.
- **Inductor losses**: Inductors contribute to losses due to their internal resistance, particularly at high switching frequencies.

6.1. Analytical Models for Power Loss Calculation

A power electronics device acting as devices (Switches) undergoes three types of modes blocking, conduction and switching mode. During blocking modes device needs to be with stand high voltage across the terminals but due to no current flow the losses are negligible. Thus the major losses occur during conduction and switching modes. Conduction Losses depends upon the forward voltage drop across switch and their internal resistance, while switching losses depends up on factors such as switching frequency, instantaneous value of drain to source current at T_{ON} and T_{OFF} instants. The switching losses evaluated for Switches are done by linear approximation of voltage and current corresponding to Switches. The power loss equation is given as:

$$P = P_{Cond} + P_{Switching}$$
 (6.1)

$$P_{Cond} = I_D^2. R_{ds}(hot). D$$
 (6.2)

Pswitch =
$$\frac{VI_D}{2}$$
 (T_{ON} + T_{OFF}). f_{sw} + C_oV² f_{sw} (6.3)

The switching and conduction losses are calculated from equation 6.2 and equation 6.3. The parameters values for the MOSFET are presented in table 6.1. The Switching and conduction losses are calculated as 2.1 mW and 1.8 mW respectively mentioned in table 6.2. Thus the total power loss of the proposed hybrid multilevel inverter is 3.9 mW.

TABLE -6.1: PARAMETERS VALUE OF POWER ELECTRONIC DEVICE (STANDARD)

S.No.	Name & Symbol	Values
	·	
1.	Drain to source Resistance-R _{ds}	4.0 m ohms
2.	On time-T _{ON}	14 ns
3.	Off time-T _{OFF}	50 ns
4.	Output capacitance-C _o	690 pf
5.	Switching frequency-f _{sw}	1KHz
6.	Duty Cycle-D	0.5
7.	Drain Current-I _D	0.3 A
8.	Forward Voltage -V	12 V

TABLE-6.2: SWITCHING & CONDUCTION LOSSES

S.No.	Losses	Value
1.	P_{Cond}	1.8 mW
2.	P _{Switching}	2.1 mW
3.	P (Total)	3.9 mW

7. Conclusion

This paper presents an in-depth investigation into the reliability and power loss characteristics of hybrid multilevel inverters for symmetrical/asymmetrical sources. The analysis shows that hybrid MLIs offer significant advantages in terms of power conversion efficiency and reliability, making them ideal for renewable energy and industrial applications. By implementing optimized switching strategies, advanced thermal management techniques, and high-efficiency semiconductors, hybrid MLIs can achieve reduced power losses and extended operational life spans. Future research should focus on further refining control algorithms and exploring new materials to enhance the performance of hybrid MLIs in emerging power conversion systems.

REFERENCES

- 1. Burla, S., Dash, R., Shukla, S. P., & Dwivedi, A. (2023, September). Improved Gravitational Search Algorithm based Hysteresis controller for Grid integrated SPV system. In 2023 IEEE 2nd International Conference on Industrial Electronics: Developments & Applications (ICIDeA) (pp. 620-624). IEEE.
- 2. Chattoraj, J., Dwivedi, A., & Pahariya, D. Y. (2017). Enhancement of power quality in SAPS system with multilevel inverter. Int. J. Eng. Sci. Res. Technol., 6(5), 779-788.
- 3. Dwivedi, A. (2012). International Journal of Engineering Sciences & Management Benefits of Standalone Power Supply System. Int. J. of Engg. Sci. & Mgmt.(IJESM), 2(1), 62-65.
- 4. Dwivedi, A., & Pahariya, Y. (2017). Design and Analysis of 1.4 MW Hybrid Saps System for Rural Electrification in Off-Grid Applications. International Journal of Energy and Power Engineering, 11(11), 1143-1147.
- 5. Dwivedi, A., & Pahariya, Y. (2018). Design of Continuous Mode Hybrid Standalone Power Station with Hybrid Controller to Select the Best Optimal Power Flow.
- 6. Dwivedi, A., & Pahariya, Y. (2021). Design and analysis of hybrid multilevel inverter for asymmetrical input voltages. Journal of Electrical Engineering & Technology, 16(6), 3025-3036.
- 7. Dwivedi, A., & Pahariya, Y. (2023). Techno-economic Feasibility Analysis of Optimized Stand-alone PV and Hybrid Energy Systems for Rural Electrification in INDIA. Journal of The Institution of Engineers (India): Series B, 104(4), 911-919.
- 8. Gautam SP, Kumar L, Gupta S (2015) Hybrid topology of symmetrical multilevel inverter using less number of devices. IET Power Electron 8(11):2125–213
- 9. Gupta KK, Ranjan A, Bhatnagar P, Kumar Sahu L, Jain S (2016) Multilevel inverter topologies with reduced device count: a review. IEEE Trans Power Electron 31(1):135–151.
- 10. Luo H, Dong Y, Li W, He X (2014) Module multilevel-clamped composited multilevel converter (M-MC2) with dual T-type modules and one diode module. Journal of Power Electron 14(6):1189–1196.
- 11. Pradeep Kumar VVS, Fernandes BG (2017) A fault tolerant single phase grid connected inverter topology with enhanced reliability for solar PV. IEEE J Emerg Sl Power Electron 5(3):1254–1262.
- 12. Rajput, A.S., Dwivedi, A., Dwivedi, P., Rajput, D.S., Pattanaik, M. (2022). Read–Write Decoupled Single-Ended 9T SRAM Cell for Low Power Embedded Applications. In: Smys, S., Bestak, R., Palanisamy, R., Kotuliak, I. (eds) Computer Networks and Inventive Communication Technologies . Lecture Notes on Data Engineering and Communications Technologies, vol 75. Springer, Singapore.