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Intelligent Energy Storage System for Standalone PV Systems: Optimizing Battery Performance with Ultra capacitors

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ABSTRACT

This paper introduces the concept of a intelligent energy storage system (IESS) due to the limitations of heterogeneous energy storage systems in providing reliable, long-term power to dynamic loads. Dynamic loads, such as induction or DC motors, draw large currents during start-up, leading to accelerated aging of battery storage systems. By integrating an ultra capacitor with battery blocks, the sudden energy demands of these loads can be met, preventing excessive strain on the batteries. The study proposes an experimental approach to explore the advantages of a IESS that combines an ultra capacitor with a battery, storing energy generated from a stand-alone photovoltaic (PV) system. The performance of this hybrid system is tested under three different load conditions, and the results are verified. A prototype setup, including a PV module, converter, control unit, and load, is developed to compare the input and output voltage and current of the inverter, both with and without ultra capacitor batteries. Results show that, battery performance is optimized and the noted reduction in the drain rate is approximatly 22% with the use of the ultracapacitor. Increasing the ultra capacitor's capacity could further reduce battery drain significantly.

Keywords: IESS (Intelligent Energy Storage System); Ultra capacitor (UC); Battery; Dynamic load; Inverter.

1. Introduction

A Intelligent Energy Storage System (IESS) incorporating Ultra Capacitors (UCs) for Stand-Alone Photovoltaic (PV) Systems combines both batteries and ultra capacitors to store and deliver energy to a stand-alone PV setup. This design addresses the limitations of traditional battery-based storage systems, which are constrained by their slower charge and discharge rates, making them less effective in supplying large amounts of power quickly[1]. In contrast, ultra capacitors can charge and discharge rapidly, making them ideal for high-power applications. In a IESS with UCs, ultra capacitors provide the high power output required, while batteries handle long-term energy

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storage. This synergy optimizes the strengths of both technologies, creating a system that is more efficient and effective than using either alone. IESS with UCs is particularly suitable for stand-alone PV systems, which are often deployed in remote areas without grid access[2,3]. These systems store energy from the PV panels during the day and supply it to the load as needed, ensuring reliable power delivery.

This work focuses on enhancing the integration of battery-ultra capacitor technology with solar PV to create a more technically advanced and cost-effective solution for various loads, including those requiring high transient currents. The approach is timely due to the growing use of solar PV systems and the increasing demand for advanced storage technologies to improve the reliability of solar energy. The potential of ultra capacitors in PV systems is validated through both simulations and hardware experiments. The hybrid system, combining batteries and ultra capacitors, offers significant advantages in terms of specific power, lifespan, operational flexibility, and adaptability to varying loads[4,5]. This stable and reliable energy production makes the technology especially useful for industrial, commercial, and rural applications. Although PV systems can function independently or as part of a hybrid setup, current battery-less systems do not fully address the issue of solar energy availability. Battery-integrated solar systems have higher availability but still fall short in meeting the power needs of dynamic loads[6,7]. This work examines how incorporating UCs improves the availability and performance of hybrid solar systems with batteries. Figure 1.1. shows the actual practical setup of IESS for optimizing the bateery performance.

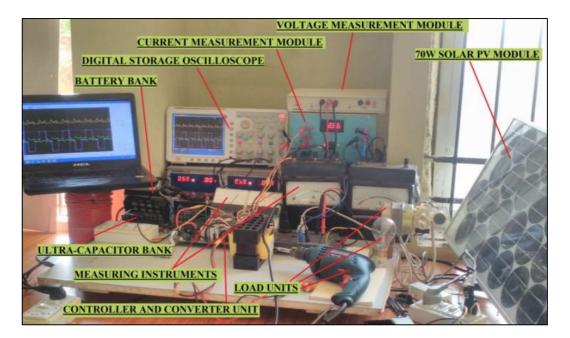


Figure 1.1:- Practical IESS System

The steps for designing and developing a Intelligient Energy Storage System (IESS) that incorporates Ultra Capacitors (UCs) are as follows:

- Determine Power Requirements: Begin by assessing the power needs of the stand-alone PV system, including the maximum output, load demands, and potential fluctuations in power due to varying light condition.
- Component Selection: Based on the identified power requirements, choose the suitable components for the IESS, such as UCs, batteries, a charge controller, inverter, and other essential components[8,9].

- **Design the IESS Control System**: Develop a control system to manage the energy flow between the UCs, batteries, and PV modules. This control system should include algorithms for Maximum Power Point Tracking (MPPT), inrush current limiting, and active power filtering [10,11].
- **Prototype and Test the IESS**: After the design is finalized, build a prototype and test it under various conditions, either in a laboratory setting or a real-world environment, to ensure it performs as expected.
- System Optimization: Based on the test results, make improvements to enhance system performance
 and efficiency. This could involve refining the component choices, control algorithms, or overall system
 configuration[12,13].
- Deploy the IESS: Once optimized and thoroughly tested, the IESS can be deployed in a stand-alone PV system, where it will help prevent large current draw during transient periods[14,15].

Thus designing and developing a IESS with UCs for stand-alone PV systems requires meticulous attention to power requirements, careful selection of components, efficient control algorithms, and rigorous testing[16]. Following these steps ensures the creation of a reliable and efficient system capable of providing stable power output under varying conditions.

1. System Configuration

The IESS setup includes a PV module, DC to DC converter, battery bank, ultra capacitor bank, uncontrolled rectifier, inverter, filter, regulator, static transfer switches (relays), AC load, and DC load. Figure 1 provides an actual setup of the IESS featuring a PV module connected to a charge controller, a battery, an ultra capacitor (UC) bank, a regulator, relay switches, a converter unit, a filter, and load. Figure 2 shows the current physical setup. In this configuration, the solar PV module captures energy from sunlight (photons) and converts it into electrical energy. The PV's output is direct current (DC), which is fed to the DC bus via a DC to DC converter. Both the battery and UC bank are connected to the DC bus through bi-directional DC to DC converters. The DC bus maintains a 24V DC power supply, and the DC loads are directly connected to this bus. For AC loads, the DC bus voltage is inverted and stepped up in the inverter section. If the PV system, battery, and UC are unavailable, the main AC line feeds an uncontrolled rectifier, which supplies DC loads and can also charge the battery and UC. When the PV system is not operational, AC loads are powered directly from the main line. The hardware setup's components are listed in Table 2.11.

The controller manages the interconnection of the various components in the energy storage system. To perform this control, it receives analog and digital inputs from voltage and current sensors and a state-of-charge detector [17,18]. The driver interprets these inputs, compares them to set values, processes them if needed, and signals output switches (relays, MOSFETs, etc.) to carry out the necessary operations. The controller used for this system is an 8-bit ATmega328 microcontroller. It monitors the availability of the public grid, the output power from the PV array, the power demand of the load, and the state of charge of the battery and UC. It compares these values with each other or with a reference value according to the control algorithm and then sends control signals to the system's output switches. Table 3.1 outlines the different operational modes of the proposed system, and Figure 3.1 provides the complete sequencing, with S_{Load}, S_{PV}, SU_{tility}, S_{Battery}, and SUC representing load power, PV array output power, grid power, battery power, and UC power, respectively.

Table 2.1 Components used in the Hardware Setup

	<u> </u>			
S.No.	Components Description	Specifications		
1.	1. Solar PV modules 70 ⁿ			
2.	Inverters	1 Phase 230 V A.C.		
3.	Solar Array Mounting System	Adjustable		

4.	DSO	10-100mhz, dual channel	
5.	Battery	12Ah, 24V	
6.	Ultra capacitors	pacitors 2.7 V	
7.	Current & Voltage Measurement Module	-	
8.	Electrical Loads (Motor, Lamp load, Etc)	Motors, Lamps	
9.	HOST PC -		
10.	Charge Controller	12A, 24 V	

1. Control Strategy

UCs are designed to operate at a low voltage of about 2.3-2.7V. In order to meet the high voltage demands, the ultra- capacitors are connected in series. In order to maintain the capacity of the UC, the series strings must be connected in parallel as shown in figure 8. As compared to an electrolytic capacitor, the energy density of an UC is 100 times larger but as compared to the lead acid battery it is much smaller. However, the power density of UC is 10 times larger than that of a lead-acid battery. UC has a fast charge-discharge capability owing to its very low internal resistance, it has a longer life cycle, it requires minimal or almost no-maintenance and it is free from emitting any matter that may prove to be harmful to the environment. The energy storage system presented uses 9 capacitors of 2.7V rating in series to attain required 24V and three such combinations are connected in parallel to get adequate Ah capacity. The UC units are thus arranged to build a UC bank which is capable to meet the demand of short-term peak load. The energy supplied by UC bank can be expressed as:

$$S_{UC} = \frac{1}{2}C(V_i^2 - V_f^2)$$

where,

 S_{UC} = Energy supplied by UC

 V_i = voltage measured initially.

V _f = voltage appearing after final discharge.

C = Capacity of UC bank.

Evaluation of UC bank Capacity.

$C = N_{ } \times \frac{C_{1_unit}}{N_{series}}$	
C = UC bank Capacity	
Where,	
$N_{ } = no. of parallel unit$	
$N_{ } = no.$ of parallel unit $C_{1_unit} = Capacity$ of one UC	
$N_{series} = no. of UC in series$	
10F	

$$C = 3 \times \frac{10F}{9} = 3.33F$$

$V_{UC_Bank} = N_{series} \times V_{1_UC}$			

Voltage of the UC bank = $9 \times 2.7V \cong 24V$

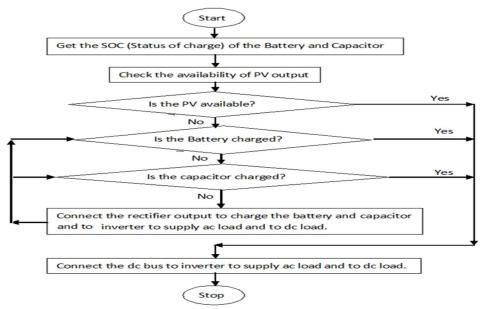


Figure-3.1:

Controller Switching Sequence Algorithm

Table 3.1 System Mode of Operation

Modes	Status of Source	System Controller Priority
Mode:1	$S_{PV} = 0$	$S_{Load} = S_{UC} + S_{Battery}$
Mode:2	$S_{UC} + S_{battery} = 0$	$S_{Load} = S_{Utility}$
Mode:3	S _{PV} , S _{Load}	$S_{Load} = S_{UC} + S_{Battery} + S_{PV}$
Mode:4	S _{PV} , S _{Load}	$S_{Load} = S_{PV}$

- In mode 2 when PV is not available then Battery and UC are both charged through utility.
- In mode 4 the excess PV is used to charge Battery and UC.

1.1.

2. Results & Discussion

2.1. Simulation Results

The performance of the IESS is evaluated using three different loads, which include a 230 V, 55 W capacitor start-run single-phase induction motor, a 60 W light bulb acting as a resistive load, and a drilling machine tool that uses an AC series motor. As the load changes, the current through the load and the voltage across the load are shown in Figure 4.1 and Figure 4.2 respectively. THD is observed to be 1.05% for load current and 1.05% across load voltage. The output current of the inverter without UC and the load current of the inverter with UC are shown in Figure 4.3. It is observed that when UC is used, the load current is almost sinusoidal.

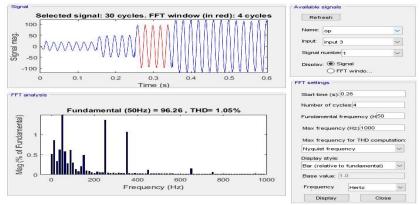


Figure 4.1: Load Current FFT

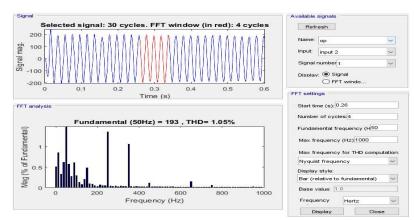


Figure 4.2: Load Voltage FFT

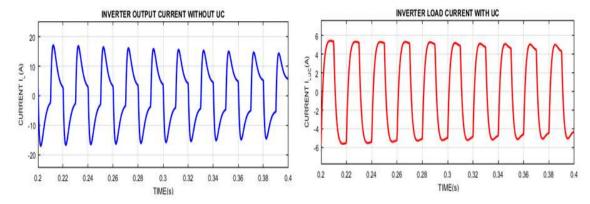


Figure 4.3: Inverter load current with and without UC.

1.1. Experimental Results

The performance of the HES system is evaluated using three different loads, which include a 230 V, 55 W capacitor start-run single-phase induction motor, a 60 W light bulb acting as a resistive load, and a drilling machine tool that uses an AC series motor. With the help of the experimental setup the input and output voltage and current waveforms with all these loads is obtained. The waveforms obtained from the DSO-TDS8204 (custom) are shown in Figures 4.4 and 4.5. A description of the signals obtained in the DSO is given in Table 4.1.

Figure 4.4 shows the variation of all quantities when a single-phase induction motor with a resistive bulb load is operated from the inverter output without a UC bank. It is clear from the current pattern that the motor initially draws a high current and then reaches a normal state; at the same time there is a voltage drop. In Figure 8, the same set of load conditions prevails, but this time the charged UC bank is connected to the battery bank

Table-4.1: Signals acquired from DSO

Channel	Quantity	Differential Probe (CT/PT)	Desired Value	Actual Value
Ch1	Inverter Input Voltage	DP252 (Scientific)	50 V	45 V
Ch2	Inverter Input Current	R00REV-0 (vibha Machatronix)	8 A	7.5A
Ch3	Inverter Output Voltage	DP252 (Scientific)	220V	200V
Ch4	Inverter Output Current	R00REV-0 (vibhaMachatronix)	5A	6 A

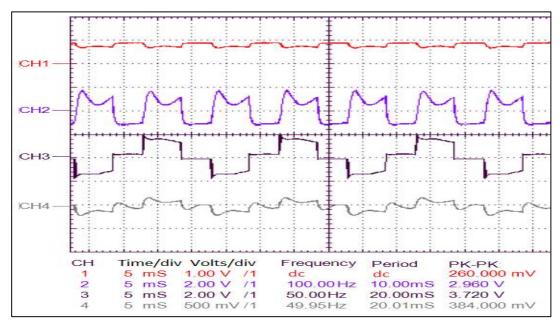
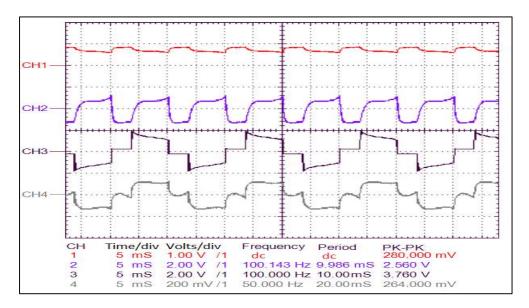


Figure-4.4: Waveforms without UC bank.

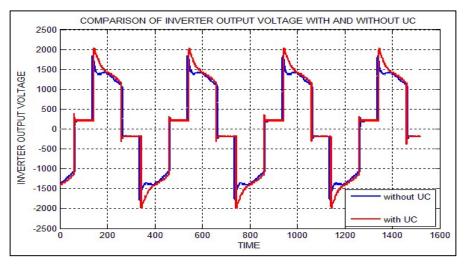
From the waveform in Figure 8, it can be easily observed that the initial rise of the waveform in the previous case





1. Figure-4.5: Waveforms with UC bank Validation of Results

Figure 4.4 and 4.5 show a comparison of waveforms on an individual basis. The MATLAB environment was used to compare two situations where the system supplies the load without UC and then with UC. The sudden drop in the initial part of the voltage wave in each cycle is limited by the UC power. This prevents the system from experiencing large voltage swings and minimizes the filter requirements on the input side of the inverter. In Figure 4.4, the current drawn by the motor has a peak value that stresses the battery and therefore the battery must undergo deep discharge cycles. With the ultra capacitor, the waveform shows a significant improvement in balancing the extremes. In Figures 4.6 and 4.7, it is possible to observe similar phenomena with the waveforms of the output voltage and current of the inverter. The output of the inverter has a quasi-square wave shape that changes with changes in the load parameters. The differential probes are used as shown in Table 4.1, the voltage and current scale is 10x and the time is in ms of the output voltage and current waveform of the inverter compared with and without the UC bank. It was observed that the inverter output current is almost the same in both simulation and experiment results.



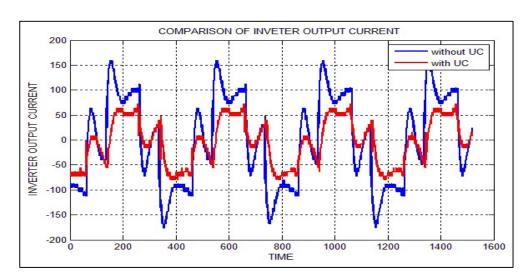


Figure-4.6: Inverter output voltage waveform comparisons with and without UC bank.

Figure-4.7: Inverter output current waveform comparisons with and without UC bank.

1. Conclusion

This work focuses on showcasing the potential of ultra capacitors (UCs) to handle sudden performance demands caused by inductive loads, particularly during start-up. The key advantage of UCs is their ability to charge and discharge at extremely high speeds, making them suitable for various high-performance applications. Due to their rapid charging and discharging capabilities, UCs can be used frequently in scenarios where high power is needed. In this study, UCs are integrated with a battery in a PV-based power system to demonstrate their effectiveness. A 60W, 230V single-phase induction motor is used as the load, and the system's performance is analyzed both with a battery alone and with a battery combined with a UC. The results show that, with a UC capacity of 3.3 Farads at 24V, battery drain is reduced by approximately 20-25%. Increasing the UC capacity further reduces battery drain significantly. These findings suggest that a higher UC capacity helps the battery operate within a more stable range. Additionally, the inverter's output voltage is kept constant during load changes through a feedback system controlling the regulator's operation. FFT analysis reveals that the harmonic distortion in the inverter's output voltage and current, with the filter unit, is 1.5%, which falls within the acceptable limit.

REFRENCES

- Dwivedi, A., Pahariya, Y. Design and Analysis of Hybrid Multilevel Inverter for Asymmetrical Input Voltages. J. Electr. Eng. Technol. 16, 3025–3036 (2021).
- 2) Luo H, Dong Y, Li W, He X (2014) Module multilevel-clamped composited multilevel converter (M-MC2) with dual T-type modules and one diode module. J Power Electron 14(6):1189–1196.
- 3) Rodriguez J, Lai J-S, Peng FZ (2002) Multilevel inverters: a survey of topologies, controls, and applications. Indus Electron IEEE Trans 49(4):724–738.
- 4) Franquelo LG, Rodriguez J, Leon JI, Kouro S, Portillo R, Prats MAM (2008) The age of multilevel converters arrives. Indus Electron Mag IEEE 2(2):28–39.
- Rodriguez KJ, Franquelo LG, Kouro S, Leon JI, Portillo RC, Prats MAM, Perez MA (2009) Multilevel converters: an enabling technology for high-power applications. Proc IEEE 97(11):1786– 1817.
- 6) De S, Banerjee D, Siva Kumar K, Gopakumar K, Ramchand R, Patel C (2011) Multilevel inverters for low-power application. IET Power Electron 4(4):384–392
- 7) Gupta KK, Ranjan A, Bhatnagar P, Kumar Sahu L, Jain S (2016) Multilevel inverter topologies with reduced device count: a review. IEEE Trans Power Electron 31(1):135–151.

- 8) Gautam SP, Kumar L, Gupta S (2015) ,Hybrid topology of symmetrical multilevel inverter using less number of devices. IET Power Electron 8(11):2125–2135
- 9) Gupta KK, Jain S (2014), A novel multilevel inverter based on switched DC sources. Indus Electron IEEE Trans 61(7):3269–3278.
- Babaei E, Laali S, Bayat Z (2015), A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches. IEEE Trans Indus Electron 62(2):922–929.
- 11) Sadigh AK, Dargahi V, Corzine KA (2015) ,New multilevel converter based on cascade connection of double flying capacitor multicell converters and its improved modulation technique. IEEE Trans Power Electron 30(12):6568–6580.
- Oskuee MRJ, Karimi M, Ravadanegh SN, Gharehpetian GB (2015), An innovative scheme of symmetric multilevel voltage source inverter with lower number of circuit devices. IEEE Trans Power Electron 62(11):6965–6973.
- Cipriano dos Santos E, Gonzaga Muniz JH, Cabral da Silva ER, Jacobina CB (2015) ,Nested multilevel topologies. IEEE Trans Power Electron 30(8):4058–4068.
- 14) Madhukar Rao A, Sivakumar K (2015) ,A fault-tolerant single-phase five-level inverter for grid-independent PV systems. IEEE Trans Indus Electron 62(12):7569–7577.
- 15) Choi U-M, Lee K-B, Blaabjerg F (2014), Diagnosis and tolerant strategy of an open-switch fault for T-type three-level inverter systems. IEEE Trans Indus Appl 50(1):495–508.
- 16) Chattopadhyay SK, Chakraborty C (2015), Performance of three-phase asymmetric cascaded bridge multilevel inverter. IEEE Trans Indus Electron 62(10):5983–5992.
- Gautam SP, Kumar L, Gupta S, Agrawal N (2017), A single phase five level inverter topology for single and multiple switches fault tolerant. IEEE Trans Power Electron 64(3):2004–2014.

Pradeep Kumar VVS, Fernandes BG (2017), A fault tolerant single phase grid connected inverter topology with enhanced reliability for solar PV. IEEE J Emerg SI P