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Design of High-Speed GNRFET-Based Analog to Digital Converter

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ABSTRACT

This work presents the design and simulation of two-, three-, and four-bit analog-to-digital converters (ADCs) utilizing Graphene Nano Ribbon Field Effect Transistors (GNRFETs). The GNRFET devices employed in this design had a channel length of 16 nm and were operated at a supply voltage of 0.7 V. Advanced Design System (ADS) was used as the simulation platform. To achieve a compact and efficient design, a current mirror topology was implemented for biasing. Each ADC configuration was evaluated in terms of power consumption. Within the 0.7 V supply voltage, the designs exhibited a full-range linear input characteristic. These results indicate that this ADC design is particularly well-suited for applications in high-speed nano-electromechanical systems (NEMS), memory cells, and advanced computing architectures. The average percentage reduction in delay is 12% for standard transistor logic (STI) and 32% for the ADC design, respectively. Additionally, power-optimized ternary logic circuits tend to operate faster.

Keywords:
Multi-Valued Logic (MVL), GNRFET, Ternary Logic Gates, STI, and ADC.

. INTRODUCTION

A common challenge in many electromechanical systems is the disparity between the speed of transmission and the availability of assembly for chemical bond formation [1]. The increasing demand for high-speed systems and smaller integrated circuits (ICs) to enhance performance has pushed the limits of traditional technologies. Scaling Complementary Metal-Oxide-Semiconductor (CMOS) technology, while widely used, has encountered significant challenges. As transistor sizes shrink, the silicon dioxide gate oxide thickness decreases, leading to increased gate capacitance and drive current. This improvement in device performance, however, is accompanied by short-channel effects that necessitate modifications in channel design. Nanotechnology offers a promising solution to overcome the limitations of conventional MOSFETs. Graphene Nanoribbon Field-Effect Transistors (GNRFETs) are a particularly promising alternative to silicon-based transistors [2]. Unlike graphene, graphene nanoribbons (GNRs) exhibit a bandgap, making them suitable for nanoscale devices with desirable ON/OFF ratios [3]. GNRs are considered one of the most promising candidates for field-effect transistor (FET) applications [4]. The transport properties of carriers in GNRFETs have been extensively studied [5]-[6]. Wide-area graphene transistors often lack coherence, and the mechanisms underlying electron pairing, influenced by electron-phonon (e-ph) scattering processes, significantly impact their electrical properties [7], [8]. As a result, even at relatively low frequencies, e-ph interactions must be considered when simulating GNRFETs [9].

The following are the contributions made by this paper:

- Describe the different electromechanical properties of a practical graphene nano-ribbon inspired transistor.
- Make a range of basic ternary logic gates with GNRFET.
- Examine current designs based on factors such as power delay product (PDP), energy consumption, and gradual delay.

1. This study expands on the foundational concept presented in [23], offering a comprehensive approach to implementing graphene nanoribbon field-effect transistor-based logic and computational circuits [24]-[27]. Section II briefly outlines the mathematical framework for a three-valued logic systems. Section III gives an explanation the operational principles of the GNRFET and demonstrates its application in circuits for three-valued logic and computation. Section IV compares the way that GNRFET-based three-valued logic circuits by those built on current technologies, assessing both qualitative and quantitative aspects. Finally, Section V concludes the study giving an overview of the main conclusions and a brief overview of the current work.

2. II. GNRFET LOGIC TERNARY SYSTEM

A digital system that employs two distinct logic levels, True (1) and False (0), is known as a binary system. Traditional binary logic, with its truth values representing true and false, can be extended into a multi-valued logic (MVL) system when R > 2, allowing for "R" distinct logic levels. A specific type of MVL system is three-valued logic, which typically uses R = 3. Three-valued logic systems can be either balanced or unbalanced, with possible logic levels such as 0, 1, 2, or -1, 0, 1. This work explores an unbalanced three-valued logic system utilizing a supply voltage (VDD) of 0.95V and ground potential (0V). Table I presents the conventions for unbalanced three-valued logic levels and their associated energy states. A general three-valued logic device for power supply (GTI) can be categorized into three types based on its operation: Negative, Positive, or Standard. Equations (1), (2), and (3) define the behavior of a Negative three-valued power supply device (NTI), a Positive three-valued power supply device (PTI), and a Standard three-valued power supply device (STI), respectively, where 'x' represents the input and 'y0', 'y1', and 'y2' represent the outputs [28].

TABLE I
THREE LOGICAL AND VALUED VOLTAGE LEVELS

Voltage	Symbol
0V	0 (False)
1/2V_{DD} (0.45V)	1 (Intermediate)
V_{DD} (0.9V)	2 (True)

TABLE II
GENUINE TABLE OF NTI, PTI & STI

Logic Input (x)	NTI(Y_0)	PTI(Y_1)	STI(Y_2)
0 (0 V)	2	2	2
1 (0.45 V)	0	2	1
2 (0.9 V)	**0**	**0**	**0**

The actual data that represent the functions y0, y1, and y2 are displayed in Table II.

$$y0 = Z0\ (x) = \begin{cases} 2, & x = 0 \\ 0, & x \neq 0 \end{cases} \quad (1)$$

$$y1 = Z1\ (x) = \begin{cases} 0, & x = 2 \\ 2, & x \neq 2 \end{cases} \quad (2)$$

$$y2 = Z2\ (x) = \bar{x} = 2 - x \quad (3)$$

A. The Importance of GNRFET

In this paper, semiconducting graphene nanoribbons (GNRs) are employed in the implementation

of the MVL design [29]. A structure featuring an armchair GNR with N dimer lines is illustrated in the Fig. 1. The number of dimer lines (N) in a GNR significantly influences its electronic properties. When N = 3p or 3p + 1, where p is the number, the GNR exhibits semiconductor characteristics [31], [32]. The width of a GNR may be determined by utilizing the following relation: (5), where $a_{c\text{-}c}$ represents the lattice constant, which is 0.142 nm.

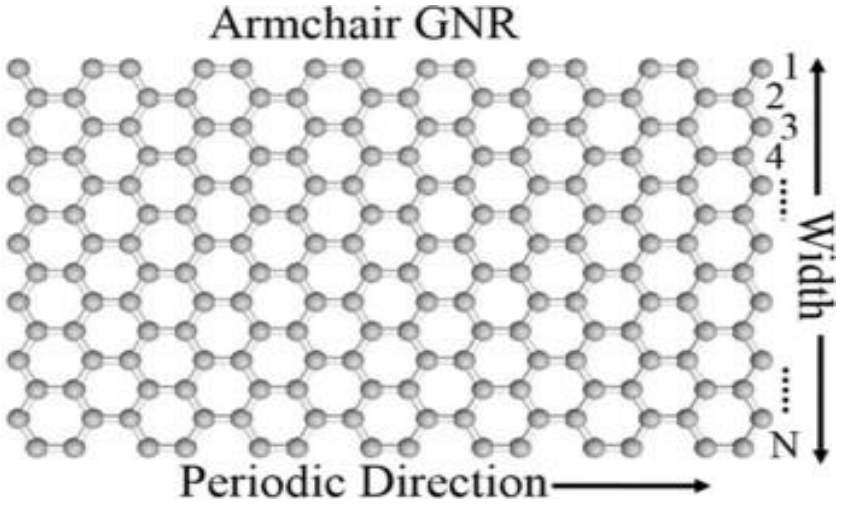


Fig. 1. Dimensions of an Armchair GNR using high-quality Dimer lines.

$$W_{GNR} = (N - 1)\frac{\sqrt{3}}{2} a_{c-c} \qquad (4)$$

To enhance driving force, resilience, and create a more extensive contact area, many ribbons running parallel to one another are utilized. This setup for the three-strip Graphene nanoribbon device is illustrated in Fig. 2. The reservoirs serve as the sections Those link the interaction and access components, and the fixing element will fix them thoroughly with $f_{dop} = 0.001$ [33]. In the figure 2, L_{ch} represents the channel length, L_{res} denotes the reservoir length, W_{ch} (WGNR) denotes ribbon width, W_{gate} denotes gate width, and $2W_{sp}$ denotes ribbon spacing. (5) [34] can be applied to determine a GNRFET's drain current.

$$I_{D} = (T_{CH}, V_D, V_S) = \frac{2qkT}{h}\sum\alpha \left[\ln\left(1 + e^{\frac{q(T_{CH} - V_S) - \varepsilon a}{kT}}\right) - \ln\left(1 + e^{\frac{q(T_{CH} - V_S) - \varepsilon a}{kT}}\right)\right] \qquad (5)$$

Here, Ψ_{CH} = Channel probable, V_S = Source Voltage, V_D = Trough voltage, ε_d = Sub band advantage, α = Sub group guide ($1 \le \alpha \le N$), k = Boltzmann incessant is the physical constant relation which is a normal kinetic dynamism of the gas atoms and temperature of the gas denoted by k or kB, h = the simple quantum for a continual action, and T = High temperature.

After a specific V_{ds}, this current shows a practically constant value, marking the start of the saturation region. The I_D versus V_{gs} curve is plotted with a foundational energy of 1.0 V. Similar to other MOS transistors, this curve provides valuable insight into the threshold power. When V_{gs} is increased beyond a specific level, the N-type GNRFET activates. Power grows in direct proportion to the increase of energy. A GNRFET can be tweaked to produce the desired threshold voltage by adjusting the dimer readings. Each transistors has a channel length of 16 nanometers.

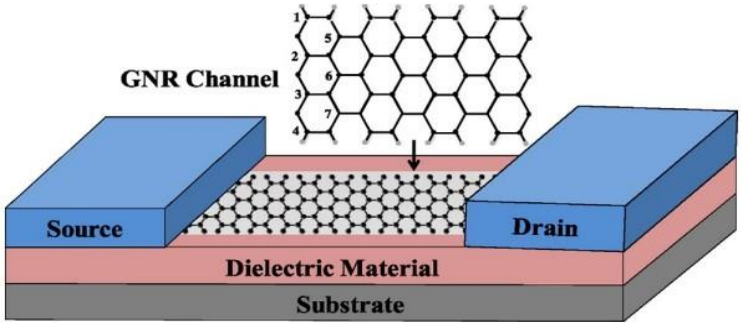


Fig. 2. A GNRFET Armchair with three (or more) ribbons [30].

B. Inverter

Figure 3 illustrates the design of a negative three-valued power supply device (NTI) alongside a positive three-valued power supply device (PTI). For the p-type and n-type GNRFETs, there are seven and nine dimer lines (N), respectively. For the PTI design, the p-type GNRFETs have N = 9, while the n-type GNRFETs have N = 7. The architecture of a conventional three-valued power supply device (STI) is depicted in Figure 4. Transistors Q4, Q5, and Q6 are p-type in this configuration, whereas transistors Q1, Q2, and Q3 have threshold voltages of -0.24 V, 0.24 V, and 0.6 V, in that order.

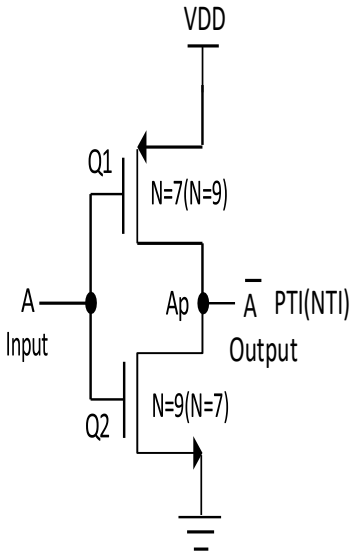


Fig. 3. Illustration of Adverse Representation (Positive) Three valuable power-producing devices.

Transistors Q1 and Q2 are configured with N = 9 and N = 7, respectively, while transistor Q3 is set to N = 10 to achieve the required threshold voltage. As soon as the input voltage is less than 0.3 V and starts to increase, transistor Q1 turns ON, producing an output voltage that is high. As the input voltage increases to a range between 0.3 V and 0.6 V, transistor Q3 turns ON while Q1 and Q2 are turned OFF. When the voltage input is within the span of 0.6 V to 0.9 V and begins to decrease, transistor Q2 turns ON, leading to a low output voltage.

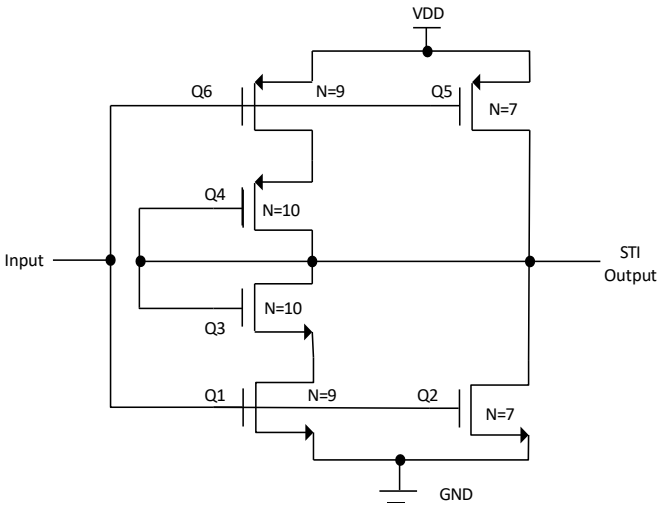


Fig. 4. Illustration of a normal Three-Valued Inverter with GNRFET representation.

3. III. Logic Design for TERNARY CIRCUITS

In this subsection we are going to describe the stranded ternary inverter and the ternary decoder circuits and will demonstrate the suggested layout with logic gates.

A. Standard Ternary Inverter (STI)

This section demonstrates an inventive STI logic gate plan as illustrated in Fig. 5. The ternary logic gates verified with CNTFET [35], this essay uses ternary logic gates verified with GNRFET.

TABLE III
GNRFET BEHAVIOUR DEPENDENCY ON DIMER LINES (N)

Dimer Lines, N	Band Gap	I_{on}/I_{off}	Order of I_{on}/I_{off}	I_{on}
8, 11, 14, 17	Small	Lowest	~10^1	Highest
6, 9, 12, 15, 18	Moderate	High	~10^6	High
7, 10, 13, 16	Highest	Highest	~10^6	Low

The circuit presented in Fig.5 has been verified with GNRFET for dimer line stipulated in table III. Because the result is logic 0 when A is logic 1 when put into practice, the transistors (Q1, Q4, and Q5) are turned ON, while the transistors (Q2 and Q3) are turned OFF. The transistor (Q3) lit up when output A made logic 2. Thus, the result is equivalent to logic 2. Transistors (Q2, Q4, and Q5) are deactivated during input time, but transistor (Q1) is enabled when A becomes logic 1.

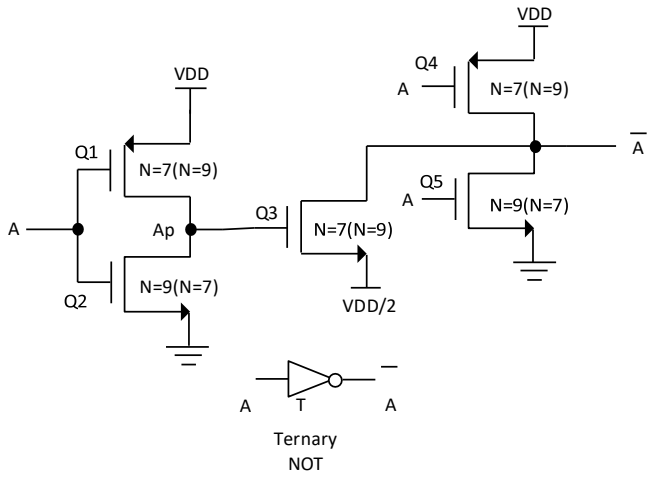


Fig. 5. The Standard Ternary Inverter circuit with GNRFET.

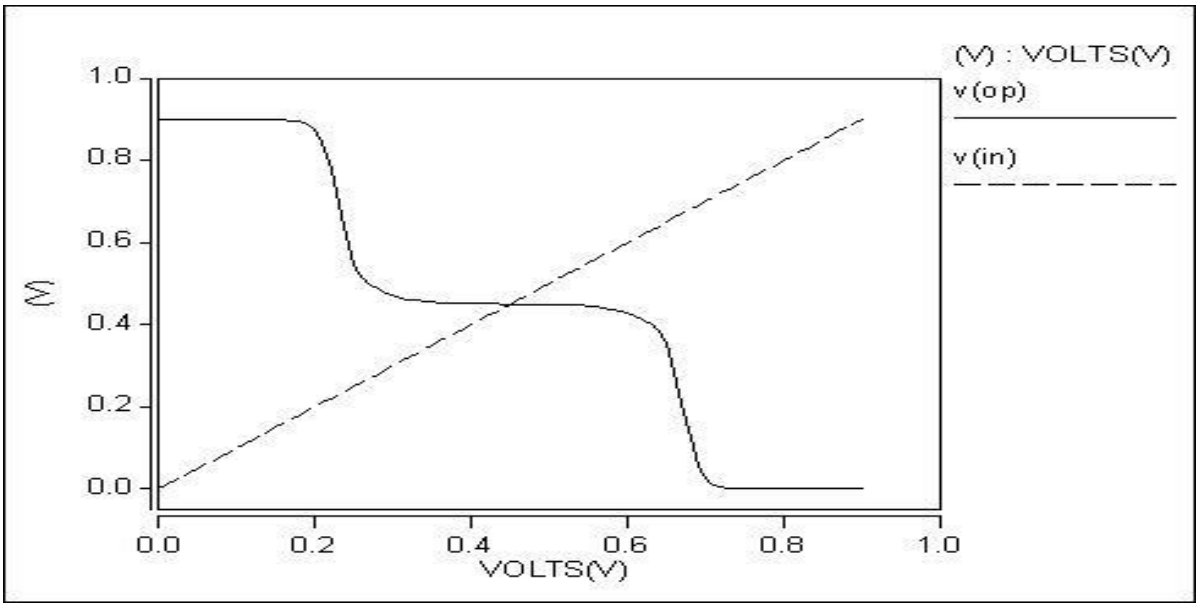


Fig. 6. Transfer curve of STI using GNTFET.

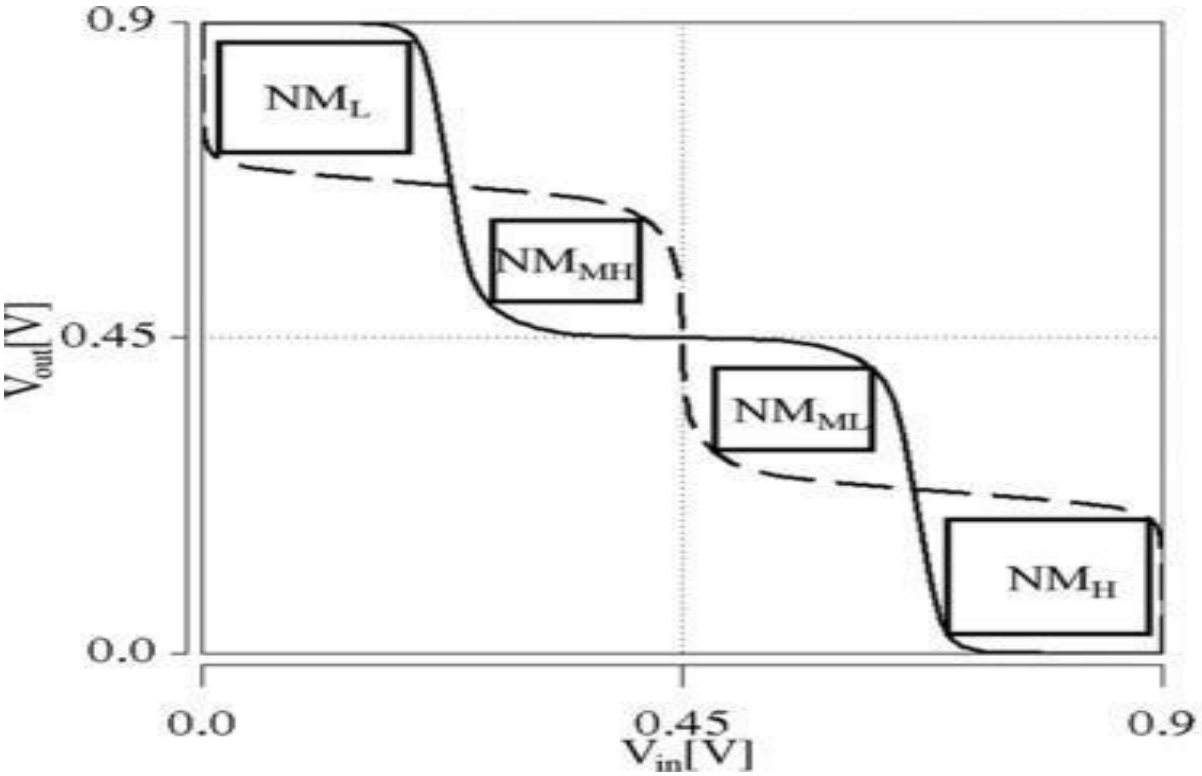


Fig. 7. The GNRFET-based STI's noise margins are displayed as butterfly curves (NM).

Transistor (Q3) is turned on when output Ap equals logic 2. The output therefore equals logic 1. Transistors (Q2, and Q5) may be switched ON at this moment of input when A becomes logic 2, whereas transistors (Q1, and Q4) may be turn OFF. The transistor (Q3) is able to be turned off when the Ap approaches logic zero. The output therefore equals logic 0. Fig. 6 displays the voltage transfer curve of the STI. It shows that the gadget can store three distinct stages of productivity energy throughout a broad spectrum. There are four distinct noise margins (NM) that impact the ternary logic circuit: (i) noise margin low (NML), (ii) noise margin low-to-medium (NMML), (iii) noise margin medium-to-

high (NMMH), and (iv) noise margin high (NMH) is shown in Fig. 7. Fig.8 displays the STI output waveforms.

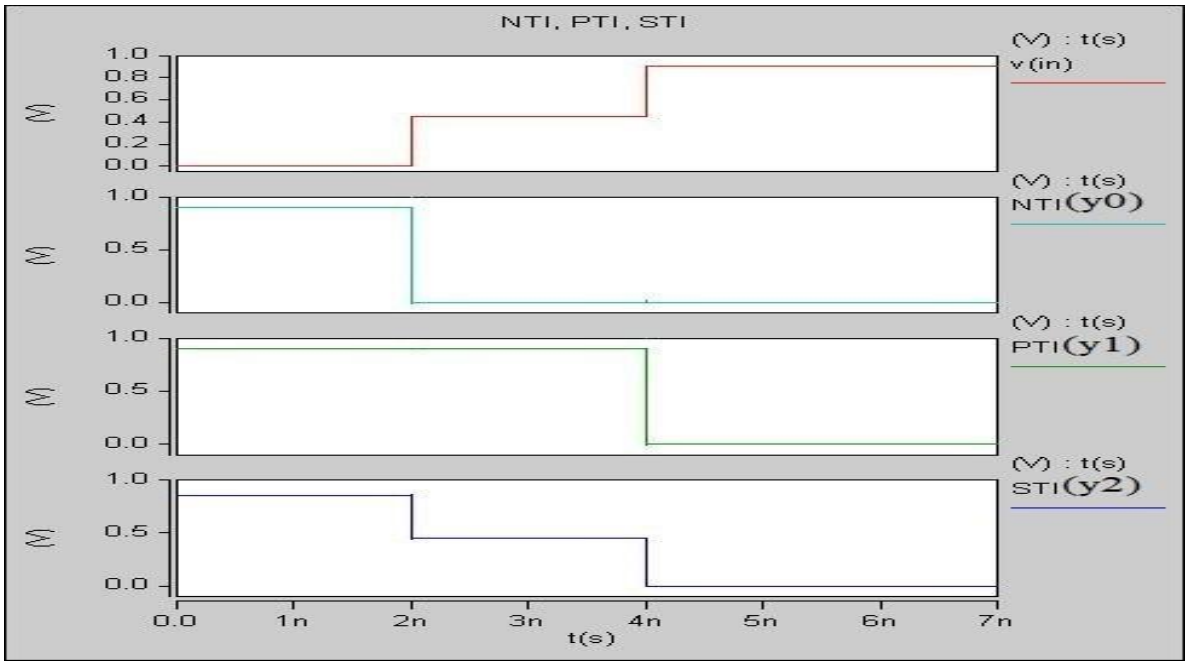


Fig. 8. The output waveforms of STI.

B. Proposed ADC

A comparator's primary function is to compare two input voltages, applied to its non-inverting and inverting terminals. This operational amplifier (Op-Amp) circuit is designed to provide a wide common-mode range and a high output swing. It achieves this by employing a differential pair of N-type transistors with their sources connected together. This design integrates both MOS and GNRFET transistors to enhance performance. A current-steering differential amplifier can be constructed using either a binary or unary structure. The binary structure is simpler than the unary structure. In a binary ADC, the sizes of the current sources vary, with the largest current source being 2^(N-1) times larger than the smallest. This significant difference in current source sizes can complicate synchronization, potentially resulting in substantial distortion and errors. Glitches and distortions at the ADC's output can significantly degrade the dynamic performance of a current-steering ADC. These glitches and distortions can arise from various factors, including the input bit decoding method, delays and misalignment among control signals, and mismatches [36]. To address delays in control signals from decoders and reduce glitch energy, the switch transistors can be placed in front of a latch circuit. This arrangement ensures that the decoder's output signals are correctly managed before the switch is activated [37].Using Static and dynamic latch circuits operating at high speeds can help manage control signals more effectively, minimizing glitches and distortions by ensuring that control signals reach the switch transistors promptly [38]. The characterization properties of the ADC devices, including Integral Non-Linearity (INL), Differential Non-Linearity (DNL), power consumption, and Signal-to-Noise Distortion Ratio (SNDR), are discussed.

TABLE IV
THE DIMER LINES, AND THRESHOLD ENERGY OF THE GNRFETS UTILIZED IN THE PROPOSED ADC

GNRFET Type	Dimer Line(N)	V_{th} (V)
P-GNRFET (Q1, Q5)	7	-0.559
P-GNRFET (Q3, Q8)	12	-0.289
N-GNRFET (Q4, Q6)	7	0.559

N-GNRFET (Q2, Q7)	12	0.289

This type of ADC can be implemented with GNRFET transistors. In the circuit design, an array of current mirrors is employed, with each mirror controlled by digital logic inputs. The switching is carried out using appropriately sized transistors. Routing the current through one of two resistors around an operational amplifier (op-amp) produces an output voltage corresponding to the digital input. The transistor switches direct the current flow, with the switch position determined by the logic value of the digital input.

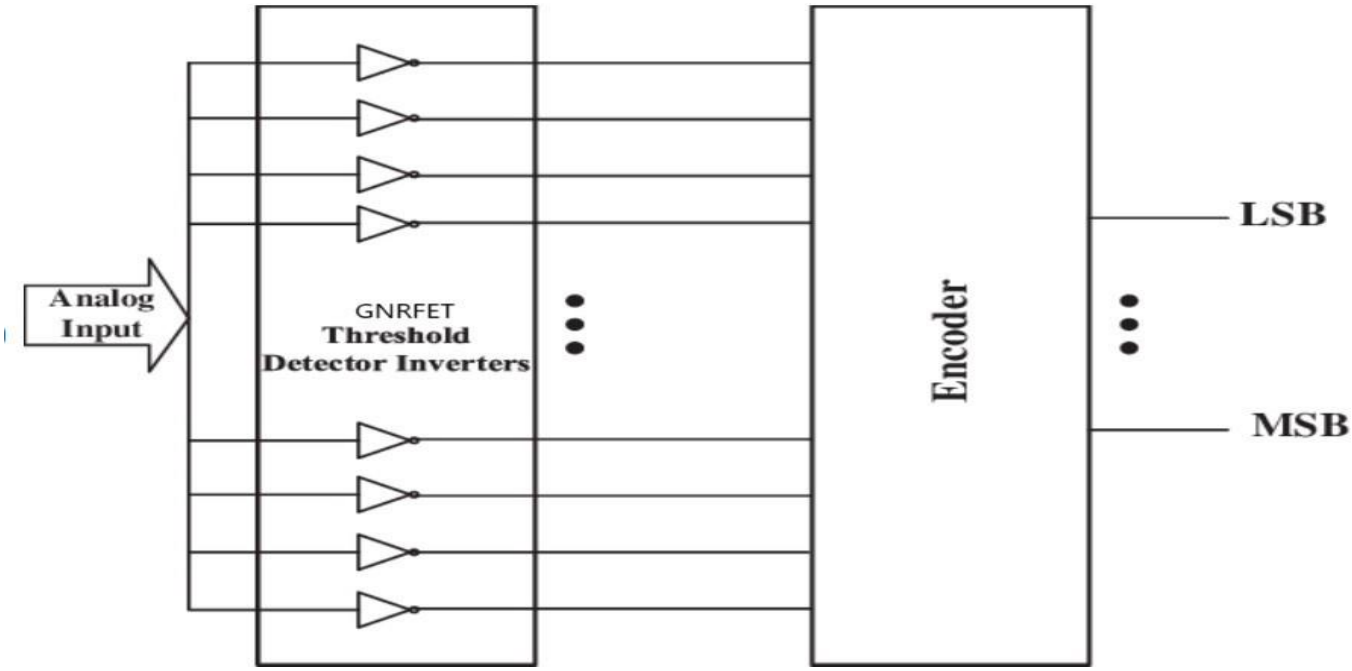


Fig. 9. The proposed GNRFET based ADC.

TABLE V
THE PROPOSED DAC DETAILED OPERATION OF FIG. 9.

Digital Input Pattern				Decimal Equivalent
a3	a2	a1	a0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

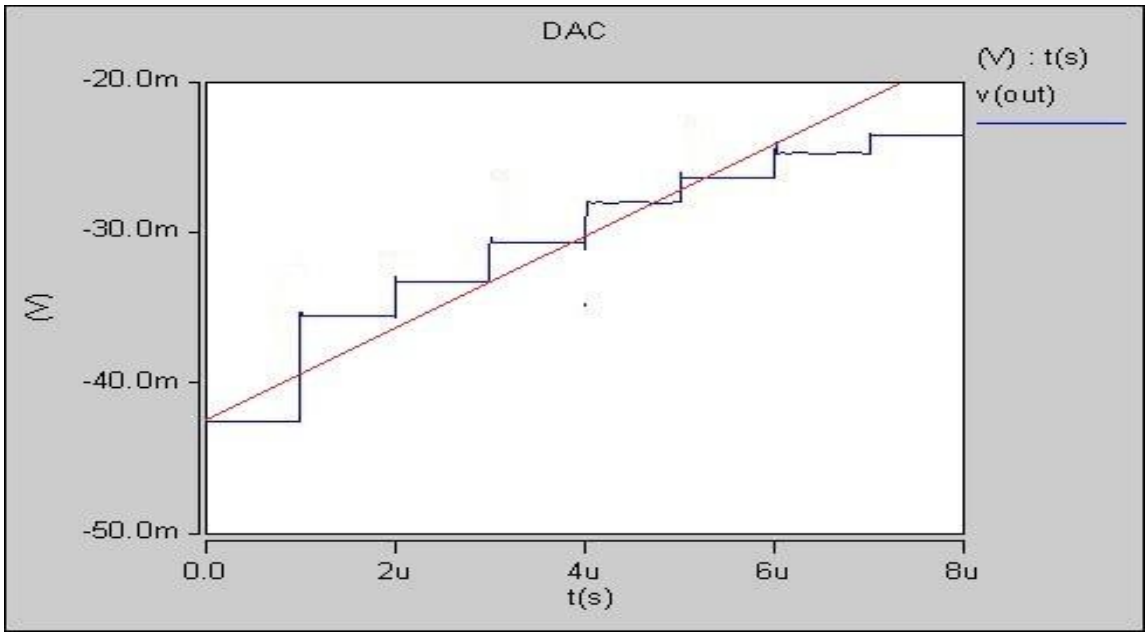


Fig.10. The proposed transient analysis of DAC.

IV. SIMULATION RESULTS OF ADC CIRCUITS

The 4-bit, 1 GS/s GNRFET-based current-steering analog-to- digital converter (ADC) was simulated using H-SPICE with a 16 nm technology node. This ADC operates on a 0.9V power supply and consumes approximately 126 μW of power. Table VI provides a comparative analysis of GNRFET with existing Carbon Nanotube Field-Effect Transistors (CNTFETs), and Table VII presents a comparison of power consumption for the ADC. The ADC exhibits monotonic behavior, meaning its output consistently increases with increasing input digital value. Table V displays the binary inputs (a3, a2, a1, and a0) ranging from '0000' to '1111' and their corresponding decimal values (0 to 15). Figure 10 illustrates the output of the current-steering ADC for these binary inputs. The results confirm that the ADC's output is static, with increasing output magnitude corresponding to increasing input digital value. The results also indicate minimal clock feed-through effects in the GNRFET-based design, unlike silicon (Si) technology, which often requires additional components to mitigate these effects. Graphene's exceptional physical properties offer the potential to significantly reduce short-channel effects observed in silicon-based devices. The GNRFET model has been validated for both digital and analog circuit applications, confirming its suitability as a fundamental building block for future CPU and GPU architectures. However, exploring various power amplifier classes and their noise performance remains a subject for future research. The devices used in this study were biased using a 0.7V supply, resulting in a very low bias current. Consequently, the electric field at the gate terminal was insufficient to induce significant carrier heating or additional stress on the devices.

TABLE VI
COMPARATIVE STUDY OF THE CURRENT CNTFET AND THE PROPOSED GNRFET – BASED TERNARY LOGISTIC GATES.

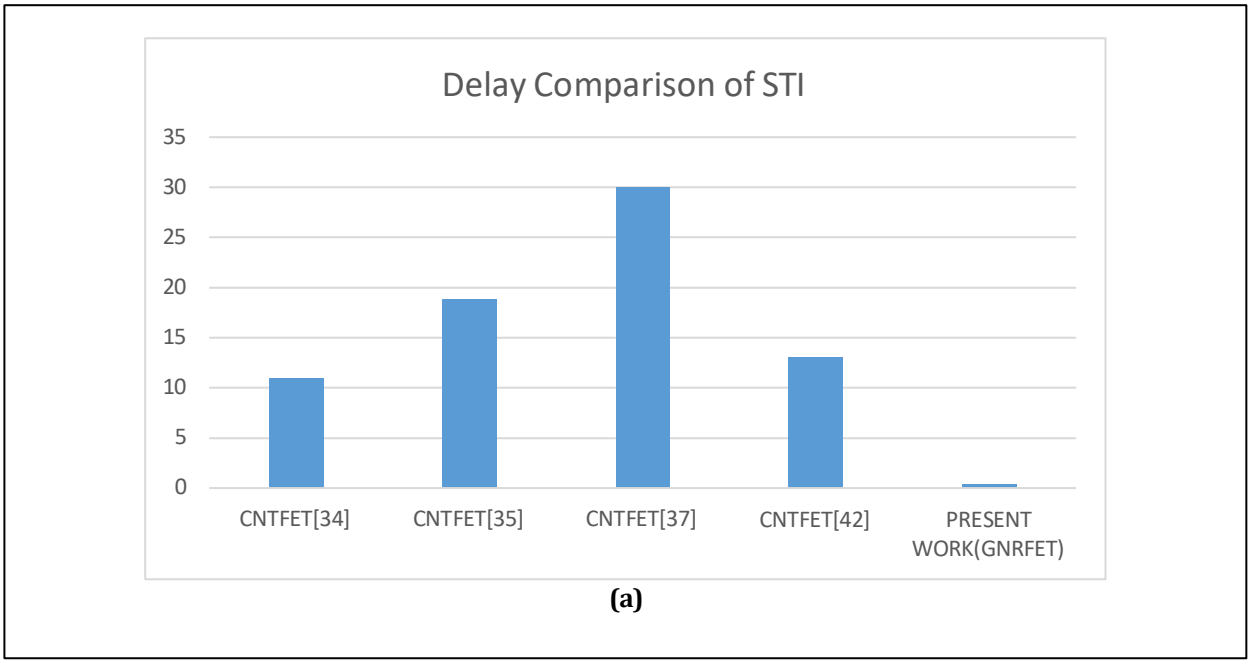
Logic Gates	Transistor count	Delay (ps)	Total Power (nW)	Power Delay Product (PDP) e-18
CNTFET [39]	6	11	88.6	0.98
CNTFET [40]	6	18.8	1170	33.2

STI	CNTFET [41]	6	30	8100	24
	GNRFET [42]	6	13	23.22	0.302
	Presented Work	5	0.38	880	0.33

TABLE VII
COMPARATIVE EVELUATION OF THE SUGGESTED GNRFET-BASED EXISTING GNRFET.

DAC device	**2 bits**	**3 bits**	**4 bits**
Power Consumption [43]	4.431 µW	4.48 µW	4.51 W
Power Consumption [Proposed]	4.11 µW	3.91 µW	3.19 W

Figures 11(a) and 11(b) illustrate the delay comparison of Standard Transistor Logic (STI) and the power consumption of the Analog-to- Digital Converter (ADC). The GNRFET-based current-steering AC exhibits a Differential Absolute Level (DAL) of 0.016 LSB, a Differential Nonlinearity (DNL) of 0.016 LSB, and an Integral Nonlinearity (INL) of 0.012 LSB, representing a substantial improvement over CMOS-based ADCs, which typically have INL values of 0.1024 LSB and DNL values of 0.1952 LSB. This paper presents a 4-bit, 1 GS/s current-steering ADC implemented using 16nm GNRFET technology.



(a)

Historically, GNRFETs have not been widely used in data converter applications. A comparison between Si-based and GNRFET-based current-

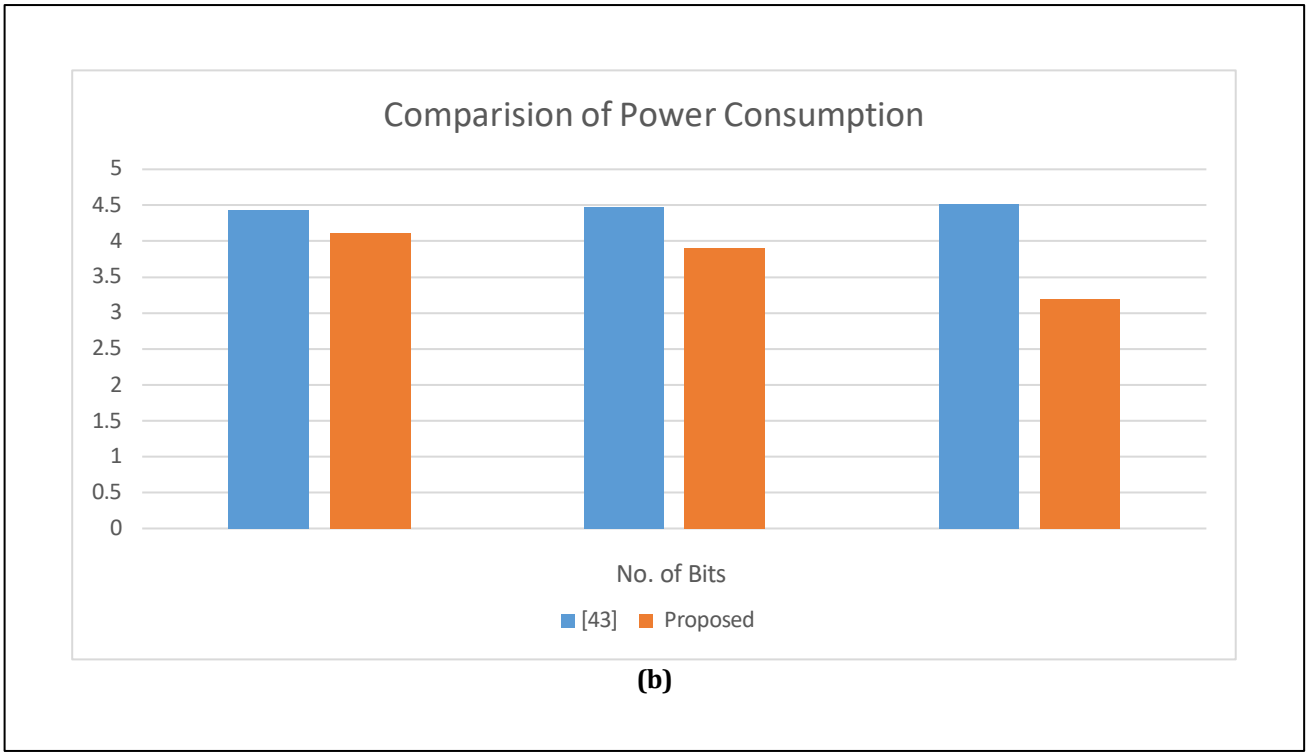


Fig. 11. The comparative transient analysis for (a) Delay of STI, (b) Power Consumption of DAC

steering digital amplifiers reveals significant advantages for the latter. In particular, GNRFET-based DACs exhibit lower power consumption, minimal clock feed-through, faster settling times, and reduced glitch energy. For example, the glitch energy of a 4-bit current-steering ADC in previous work was 2.64 pV·s, whereas in this study, it is reduced to 0.13 pV·s. These results demonstrate the superior performance of GNRFET technology and its promising potential for both ADC and DAC designs. Further investigation is necessary to assess the scalability of GNRFET-based ADCs and their integration with other advanced technologies. Additionally, long-term reliability studies and real-world testing will be crucial to validate the simulation results.

V. CONCLUSION

This research focuses on optimizing the performance and energy efficiency of a Standard Ternary Inverter and a novel Ternary Decoder implemented using Graphene Nanoribbon Field-Effect Transistors (GNRFETs). These circuits were simulated using the HSPICE tool with a 16nm technology node, a 0.9V supply voltage, and a middle voltage of 0.45V. The simulation results compared the power consumption and delay performance of ternary logic modules implemented using GNRFETs. The results demonstrate that GNRFETs offer superior power efficiency and reduced delay compared to traditional silicon-based transistors. Both gate-level and circuit-level implementations of ternary logic using GNRFETs showed significant improvements in delay and power consumption. Consequently, these circuits are well-suited for reducing battery usage in low-power portable devices and integrated systems. The simulation results also indicate that GNRFET-based Analog-to-Digital Converters (ADCs) significantly outperform traditional silicon CMOS designs in terms of speed, power efficiency, and overall performance metrics. These advancements make GNRFET-based ADCs suitable for high-speed and low-power applications, such as digital signal processing, display electronics, and data acquisition systems.

Data Availability Statement: The datasets used and/or analysed during the current study available from the corresponding author on reasonable request.

Acknowledgment: Not Applicable.

Conflicts of Interest: Authors stated that no conflict of Interest.

REFERENCES

[1] W. Zhang, C. Basaran, and T. Ragab, "Impact of geometry on transport properties of armchair graphene nanoribbon heterojunction," *Carbon N. Y.*, vol. 124, pp. 422–428, Nov. 2017, doi: 10.1016/j.carbon.2017.09.005.

[2] S. S. Ghoreishi, R. Yousefi, K. Saghafi, and H. Aderang, "A numerical study of the nanoribbon field-effect transistors under the ballistic and dissipative transport," *Int. Nano Lett.*, vol. 7, no. 3, pp. 225–232, Sep. 2017, doi: 10.1007/s40089-017-0219-x.

[3] IEEE Staff and IEEE Staff, *Graphene Nanoribbon Field-effect Transistors-2008.pdf*. 2008.

[4] M. S. Fahad, A. Srivastava, A. K. Sharma, and C. Mayberry, "Analytical current transport modeling of graphene nanoribbon tunnel field-effect transistors for digital circuit design," *IEEE Trans. Nanotechnol.*, vol. 15, no. 1, pp. 39–50, Jan. 2016, doi: 10.1109/TNANO.2015.2496158.

[5] S. S. Ghoreishi, K. Saghafi, R. Yousefi, and M. K. Moravvej-Farshi, "Graphene nanoribbon tunnel field effect transistor with lightly doped drain: Numerical simulations," *Superlattices Microstruct.*, vol. 75, pp. 245–256, 2014, doi: 10.1016/j.spmi.2014.07.042.

[6] A. Naderi, "Theoretical analysis of a novel dual gate metal-graphene nanoribbon field effect transistor," *Mater. Sci. Semicond. Process.*, vol. 31, pp. 223–228, 2015, doi: 10.1016/j.mssp.2014.11.051.

[7] P. Moslehi-Nejad, A. Shahhoseini, and B. Behtoee, "A 10-bit I-GS/s current-steering DAC with Carbon Nanotube Field Effect transistor (CNFET)."

[8] S. S. Ghoreishi, K. Saghafi, and M. K. Moravvej-Farshi, "A novel graphene nano-ribbon field effect transistor with Schottky tunneling drain and ohmic tunneling source," *Mod. Phys. Lett. B*, vol. 27, no. 26, Oct. 2013, doi: 10.1142/S0217984913501893.

[9] Y. Ouyang, Y. Yoon, and J. Guo, "Scaling behaviors of graphene nanoribbon FETs: A three-dimensional quantum simulation study," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2223–2231, Sep. 2007, doi: 10.1109/TED.2007.902692.

[10] K. C. Smith, "The Prospects for Multivalued Logic: A Technology and Applications View," 1981. doi: 10.1109/TC.1981.1675860.

[11] IEEE Nanotechnology Council and Institute of Electrical and Electronics Engineers, *Enabling Energy-Efficient Ternary Logic Gates using CNFETs Sepehr*. 2017.

[12] A. Heung and H. T. Mouftah, "Depletion/Enhancement CMOS For a Low Power Family of Three-Valued Logic Circuits," *IEEE J. Solid-State Circuits*, vol. 20, no. 2, pp. 609–616, 1985, doi: 10.1109/JSSC.1985.1052354.

[13] Y. Yoon, G. Fiori, S. Hong, G. Iannaccone, and J. Guo, "Performance comparison of graphene nanoribbon FETs with Schottky contacts and doped reservoirs," *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2314–2323, 2008, doi: 10.1109/TED.2008.928021.

[14] P. C. Balla and A. Antoniou, "Low Power Dissipation MOS Ternary Logic Family," *IEEE J. Solid-State Circuits*, vol. 19, no. 5, pp. 739–749, 1984, doi: 10.1109/JSSC.1984.1052216.

[15] A. Raychowdhury and K. Roy, "Carbon-nanotube-based voltage-mode multiple-valued logic design," *IEEE Trans. Nanotechnol.*, vol. 4, no. 2, pp. 168–179, Mar. 2005, doi: 10.1109/TNANO.2004.842068.

[16] S. Karmakar, J. A. Chandy, and F. C. Jain, "Design of ternary logic combinational circuits based on quantum dot gate FETs," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 21, no. 5, pp. 793–806, 2013, doi: 10.1109/TVLSI.2012.2198248.

[17] G. K. Johnsen, "An introduction to the memristor - A valuable circuit element in bioelectricity and bioimpedance," *J. Electr. Bioimpedance*, vol. 3, no. 1, pp. 20–28, 2012, doi: 10.5617/jeb.305.

[18] R. A. Jaber, A. Kassem, A. M. El-Hajj, L. A. El-Nimri, and A. M. Haidar, "High-Performance and Energy-Efficient CNFET-Based Designs for Ternary Logic Circuits," *IEEE Access*, vol. 7, pp. 93871–93886, 2019, doi: 10.1109/ACCESS.2019.2928251.

[19] R. A. Jaber, A. M. El-Hajj, A. Kassem, L. A. Nimri, and A. M. Haidar, "CNFET-based designs of Ternary Half-Adder using a novel 'decoder-less' ternary multiplexer based on unary operators," *Microelectronics J.*, vol. 96, Feb. 2020, doi: 10.1016/j.mejo.2019.104698.

[20] Z. Chen, Y. M. Lin, M. J. Rooks, and P. Avouris, "Graphene nano-ribbon electronics," *Phys. E Low-Dimensional Syst. Nanostructures*, vol. 40, no. 2, pp. 228–232, Dec. 2007, doi: 10.1016/j.physe.2007.06.020.

[21] X. Wang and H. Dai, "Etching and narrowing of graphene from the edges," *Nat. Chem.*, vol. 2, no. 8, pp. 661–665, Aug. 2010, doi: 10.1038/nchem.719.

[22] X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, "Chemically derived, ultrasmooth graphene nanoribbon semiconductors," *Science (80-.).*, vol. 319, no. 5867, pp. 1229–1232, Feb. 2008, doi: 10.1126/science.1150878.

[23] J. Cai *et al.*, "Atomically precise bottom-up fabrication of graphene nanoribbons," *Nature*, vol. 466, no. 7305, pp. 470–473, Jul. 2010, doi: 10.1038/nature09211.

[24] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, "Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors," *Phys. Rev. Lett.*, vol. 100, no. 20, May 2008, doi: 10.1103/PhysRevLett.100.206803.

[25] L. Jiao, L. Zhang, L. Ding, J. Liu, and H. Dai, "Aligned graphene nanoribbons and crossbars from unzipped carbon nanotubes," *Nano Res.*, vol. 3, no. 6, pp. 387–394, 2010, doi: 10.1007/s12274-010-1043-z.

[26] Z. T. Sandhie, F. Uddin Ahmed, and M. Chowdhury, "GNRFET based Ternary Logic - Prospects and Potential Implementation," Feb. 2020. doi: 10.1109/LASCAS45839.2020.9069028.

[27] A. Dhande and V. Ingole, "Design And Implementation Of 2 Bit Ternary ALU Slice," 2005.

[28] E. P. D. Chen, S. Chilstedt, C. Dong, "What Everyone Needs to Know about Carbon-Based Nanocircuits," 2010. [Online]. Available: www.dac.com

[29] M. Y. Han, B. Özyilmaz, Y. Zhang, and P. Kim, "Energy band-gap engineering of graphene nanoribbons," *Phys. Rev. Lett.*, vol. 98, no. 20, May 2007, doi: 10.1103/PhysRevLett.98.206805.

[30] Y. Y. Chen *et al.*, "A SPICE-Compatible Model of MOS-Type Graphene Nano-Ribbon Field-Effect Transistors Enabling

Gate- and Circuit-Level Delay and Power Analysis under Process Variation," *IEEE Trans. Nanotechnol.*, vol. 14, no. 6, pp. 1068–1082, Nov. 2015, doi: 10.1109/TNANO.2015.2469647.
[31] M. T. Ahmadi, Z. Johari, D. C. Y. Chek, N. A. Amin, and R. Ismail, "Modelling of graphene nanoribbon Fermi energy," *J. Nanomater.*, vol. 2010, 2010, doi: 10.1155/2010/909347.
[32] Y. W. Son, M. L. Cohen, and S. G. Louie, "Energy gaps in graphene nanoribbons," *Phys. Rev. Lett.*, vol. 97, no. 21, 2006, doi: 10.1103/PhysRevLett.97.216803.
[33] Y. Chen, "Graphene Nano-Ribbon And Transition Metal Dichalcogenide Field-Effect Transistor Modeling And Circuit Simulation," 2015.
[34] S. Lin, Y. Bin Kim, and F. Lombardi, "CNTFET-based design of ternary logic gates and arithmetic circuits," *IEEE Trans. Nanotechnol.*, vol. 10, no. 2, pp. 217–225, Mar. 2011, doi: 10.1109/TNANO.2009.2036845.
[35] S. Tabrizchi, F. Sharifi, A.- H. Badawy, and Z. M. Saifullah, "Enabling energy-efficient ternary logic gates using CNFETs," in Proc. IEEE 17th Int. Conf. Nanotechnol., 2017, pp. 542–547.
[36] B. Shukla *et al.*, *Proceedings - 2014 3rd International Conference on Reliability, Infocom Technologies and Optimization: Trends and Future Directions, ICRITO 2014*. 2015.
[37] Badugu Divya Madhuri and S. Sunithamani, "Design of Ternary D-latch Using Graphene Nanoribbon Field Effect Transistor," in *2019 International Conference on Vision Towards Emerging Trends in Communication and Networking (ViTECoN)*, 2018.
[38] D. G. Anil, Y. Bai, and Y. Choi, "Performance evaluation of ternary computation in SRAM design using graphene nanoribbon field effect transistors," in *2018 IEEE 8th Annual Computing and Communication Workshop and Conference, CCWC 2018*, Feb. 2018, vol. 2018-Janua, pp. 382–388. doi: 10.1109/CCWC.2018.8301723.
[39] R. Faghih Mirzaee, K. Navi, and N. Bagherzadeh, "High-efficient circuits for ternary addition," *VLSI Des.*, vol. 2014, 2014, doi: 10.1155/2014/534587.
[40] S. P. P. and M. B. S. Chetan Vudadha, *Proceedings - 2017 IEEE International Symposium on Nanoelectronic and Information Systems, iNIS 2017*, vol. 2018-Febru. IEEE, 2018.
[41] M. H. Moaiyeri, A. Doostaregan, and K. Navi, "Design of energy-efficient and robust ternary circuits for nanotechnology," *IET Circuits, Devices Syst.*, vol. 5, no. 4, pp. 285–296, Jul. 2011, doi: 10.1049/iet-cds.2010.0340.
[42] Z. Tasnim, S. Student, F. Uddin, and A. Student, "Design of Ternary Logic and Arithmetic Circuits Using GNRFET," no. July, 2020, doi: 10.1109/OJNANO.2020.3020567.
[43] M. Patnala, T. Ytterdal, and M. Rizkalla, "High Speed-Low Power GNRFET based Digital to Analog Converters for ULSI applications," *Proc. IEEE Natl. Aerosp. Electron. Conf. NAECON*, vol. 2019-July, pp. 451–457, 2019, doi: 10.1109/NAECON46414.2019.9057977.

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