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STUDY OF SILICON NANOWIRE FIELD EFFECT TRANSISTOR WITH DIFFERENT OXIDE MATERIAL USING FETTOY SIMULATOR

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Abstract

As the MOSFET gate length enters the nanometer regime, short channel effects (SCE) such as threshold voltage (V_T) roll off and drain- induced- barrier- lowering becomes increasingly significant, which limits the scaling capability of planar bulk or silicon-on-insulator (SOI) MOSFET. At the same time the relatively low carrier mobility in silicon may also degrade the MOSFET device performance. For these reasons, various novel device structures and materials such as silicon nanowire transistors, carbon nanotubes, new channel materials, molecular transistors are being extensively explored. Among all these, promising post CMOS structures, the silicon nanowire transistor (SNWT) has its unique advantage – The SNWT is based on silicon a material that the semiconductor industry has been working on for over forty years; it would be really attractive to stay on silicon and also achieve good device matrices that nano-electronics provides. The main objective of this paper is to present Simulation of silicon Nanowire field Effect Transistor (SNWFET) with different oxide having different k value and observe the effect on characteristics thereon using Fettoy Simulator.

Keywords: Silicon Nanowire; FET; CMOS; Dielectric Constant.

INTRODUCTION

Si nanowire FET (SNWFET) is considered as one of the promising candidate for further extending the device downsizing, owing to its gate-all-around (GAA) structure whichenables better gate control capability than planar transistor [1]. Fig 1 and Fig 2 shows schematic of GAA structure. Si-nanowire FETs have already been obtained higher I_{on}/I_{off} ratio than any planner transistor.

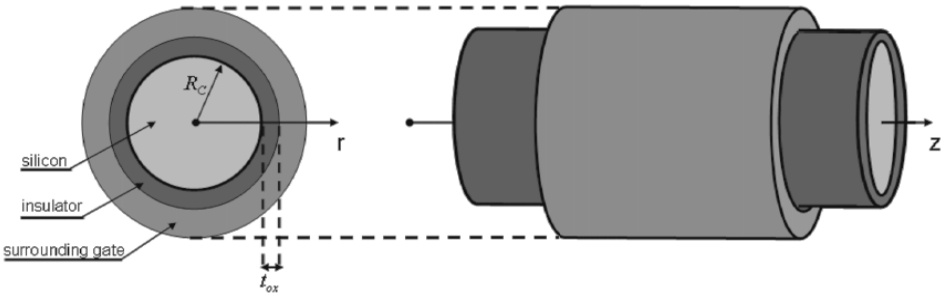

Fig. 1: Cross section View of Silicon nanowire transistors

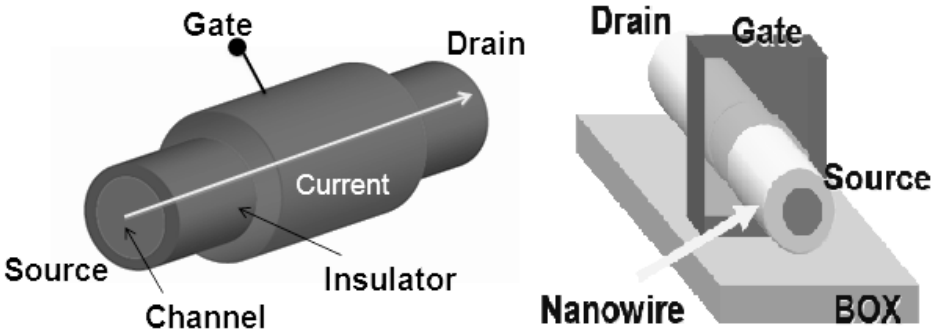

Fig. 2: Gate all around (GAA) Silicon nanowire transistors

TRANSPORT OF ELECTRONS IN NANOWIRE

Electron transport phenomenon in low dimensional system can be roughly divide into two categories:
(a) Ballistic transport
(b) Diffusion transport

A ballistic transport phenomenon occurs when electron travels along nanowire without any scattering [2]. Ballistic transport is usually observed in very short quantum wires in which electron mean free path is much larger than wire length and the condition is a pure quantum phenomenon.

In nanowire with length much larger than carrier mean free path, the electron or holes undergo numerous scattering events when they travel along the wire. In this case the transport occurs through diffusion mechanism [3]. The conduction is dominated by carrier scattering within the wire due to phonons (lattice vibration) boundary scattering, lattice and other structural defects and impurity atom.

MODELING

The modeling of ballistic FET is presented in this section, which correctly capturesquantum confinement, two-dimensional (2D) electrostatics and bias charge. It generalizes Natori model

[4] by treating 2D electrostatics and by properly treating the 1D electrostatics – even in quantum capacitance limit, where the gate insulator capacitance is much greater than the semiconductor capacitance. Itconsists of three capacitors C_G, C_S and C_D which describe the electrostatic coupling between the top of the barrier and the gate, the source and the drain respectively. The potential at the top of the barrier is obtained as:

$$U_{sfc} = \frac{C_G}{C_G+C_D+C_S} V_G + \frac{C_D}{C_G+C_D+C_S} V_D + \frac{C_S}{C_G+C_D+C_S} V_S + \frac{\theta_{Top}}{C_G+C_D+C_S} \qquad (1)$$

Where V_G,V_S and V_D are the applied bias at the gate, source and drain respectively. θ_{Top} is the mobile charge at the top of the barrier.

In the work, which is presented in this paper, the model given in equation (1) is modified to simulate ballistic nanowire transistor. Compared to a planner double-gate MOSFET, a nanowire FET has two major differences that are considered in this simulation:

(I) For a planer double-gate MOSFET, the gate oxide capacitance C_G is analytically obtained as:

$$C_G = \frac{2k\varepsilon_0}{T_{ox}} \qquad (2)$$

Where, k is the oxide dielectric constant, $\varepsilon_0$is the permittivity of vacuum and T_{OX} is the oxide thickness. For a nanowire FET, however, the gate oxide capacitance does not have an analytical expression in general, so it should be numerically computed by solving a 2D Poisson's equation at the cross-section of the SNWT. In this section, we assume coaxial gate geometry for which the gate oxide capacitance C_G can be analytically obtained as:

$$C_G = \frac{2\pi k\varepsilon_0}{\ln(\frac{2Tox+T_{si}}{T_{si}})} \qquad (3)$$

Where, T_{si} in the thickness of silicon body.

(II) Due to the one dimensional E-K relations for a nanowire FET the equation for the SNWT charge density and current are different from those for 2D planer MOSFETs. To be specific, the mobile charge to the Top of the barrier is obtained as:

$$\theta_{Top} = -q(n^+ + n^-) = -\frac{qN_{1D}}{2}\vartheta_{-1/2}(\eta_F) - \frac{qN_{1D}}{2}\vartheta_{-1/2}(\eta_F) \qquad (4)$$

Where q is the charge on electron and

$$N_{1D} = M\sqrt{\frac{2K_BTm_x^*}{\pi\hbar^2}} \qquad (5)$$

m_x^* is the effective-mass of electron in the transport direction, $\hbar$ is plank constant , K_B is Boltzmann's Constant, T is the ambient temperature and M is the valley degeneracy (for a cylindrical SNWT with <100> oriented channel, M = 4 and $m_x^* = 0.19\ m_e$, where m_e is the free electron mass), and

$$\eta_F = \frac{\mu_s-(\varepsilon(0)-qU_{scf})}{K_BT} \qquad (6)$$

Where,μ_s is the source Fermi level and $\varepsilon(0)$ represents the lowest sub band level at the top of the barrier when $U_{scf} = 0$.
U_D in equation (4) is defined by:

$U_D = \frac{V_{DS}}{K_B T}$ (7)

Where $V_{DS} = V_D - V_S$ is the applied drain bias. The function $\vartheta_j(\eta)$ is called Fermi integral which is defined as

$\vartheta_j(\eta) = \frac{1}{\lceil(j+1)} \int_0^\infty \frac{x^j dx}{1+\exp(x-\eta)}$ (8)

Similarly, the electron current for a nanowire FET can be analytically expressed as:

$I = I^+ - I^- = M\frac{qK_BT}{\pi\hbar} [\vartheta_0(\eta_F) - \vartheta_0(\eta_F - U_D)]$

$= M\frac{qK_BT}{\pi\hbar} \ln\left(\frac{1+e^{\eta_F}}{1+e^{\eta_F - U_D}}\right)$ (9)

Below mentioned are the basic assumptions that are made in this analytical approach:

(I). Coaxial gate geometry is assumed and quantum confinement is neglectedto obtain an analytical expression ofthe gate oxide capacitance. In general, to evaluate the gate oxide capacitance for an arbitrary SNWT structure with the consideration of quantum confinement, which keeps the electron charge centroid somehow away from the Si/Sio2 interfaces, a2D Poisson's equation need to be numerically solved togetherwith a 2D Schrodinger equation.

(II). For nanowire FET with thicker bodies, multiple sub band should be considered. As described in [6], this simple analytical model can be easily extended to include multi-sub bands in the calculation of mobile charge density and terminal current.

(III). This simple analytical model is based on a semi classical ballistic transport model , In which the quantum mechanical tunneling from the source to the drain is not considered. According to [7] source-to-drain tunneling may not be important when the channel length of the FET is>8 nm, especially for the ON- state. Therefore, asemi classical ballistic transport model is well acceptable in this simple analytical simulation.

SIMULATION OF 1D NANOWIRE FET

In this section, the simulation of ballistic nanowire FET using simple analytical approach described in section 3 is presented. A coaxial gate geometry configuration is assumed and <100> orientation is taken so the valley degeneracy is M=4(i.e. four unprimed valley, [010],[0$\bar{1}$0] ,[001] and [00$\bar{1}$] are degenerate) and the longitudinal effective mass $m_x^* = 0.19\ m_e$. A hypothetical thin silicon body T_{si}=1nm, is selected to guarantee only lowest sub band at each valley is occupied. Moreover, we assume the oxide layer thickness T_{ox}= 1.5 nm and two oxides having dielectric constant k=3.9 for Sio_2 and k=20 for HFO_2 (Hafnium Oxide) which is selected to illustrate the full degenerate and quantum capacitance effects in nanowire FETs. To capture the 3D electrostatics in the simulated nanowire FETs, we assume that:

$\alpha_G = \frac{C_G}{C_G+C_D+C_S} = 0.88$; $\alpha_D = \frac{C_D}{C_G+C_D+C_S} = 0.035$ (10)

I-V Characteristics: Fig 3 (a) shows the plot of I_DVs V_{GS} transfer characteristics and fig 3(b) shows output characteristics, i.e, I_DVs V_{DS} of the simulated SNWFET with SiO_2 layer as dielectric having K=3.9

Fig 4(a) is same plot for SNWFET with HFO_2 insulator having K=20. It is observed from these plots that for K=3.9 the channel conductance increases with gate voltage while for K=20, it saturates when the gate voltage is sufficiently high.

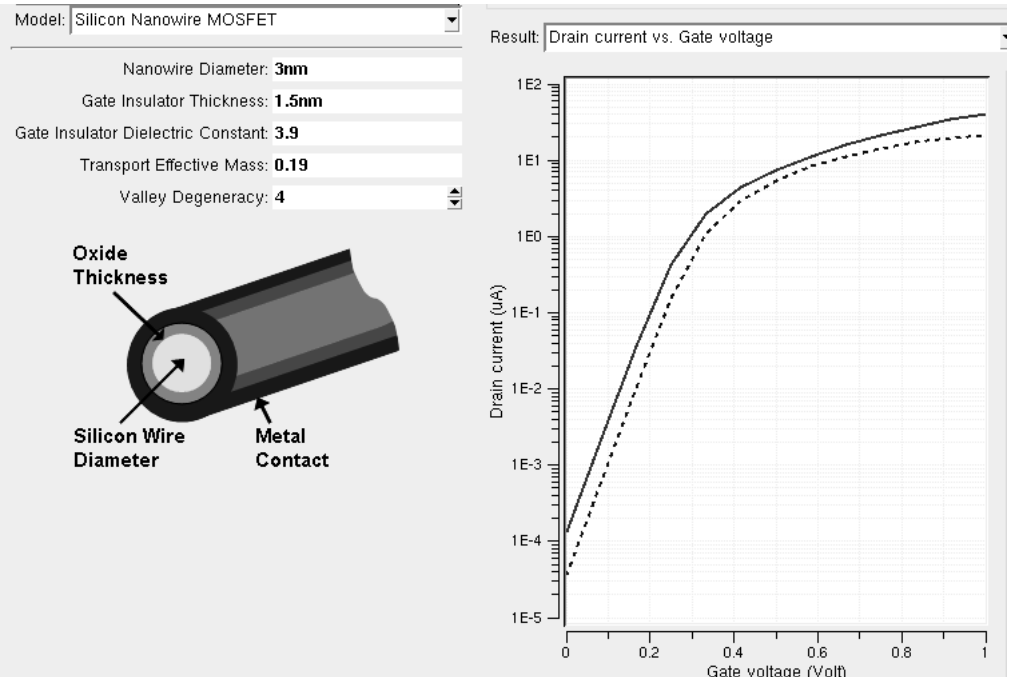

Fig. 3a: log I_DVs V_{GS} for k =3.9

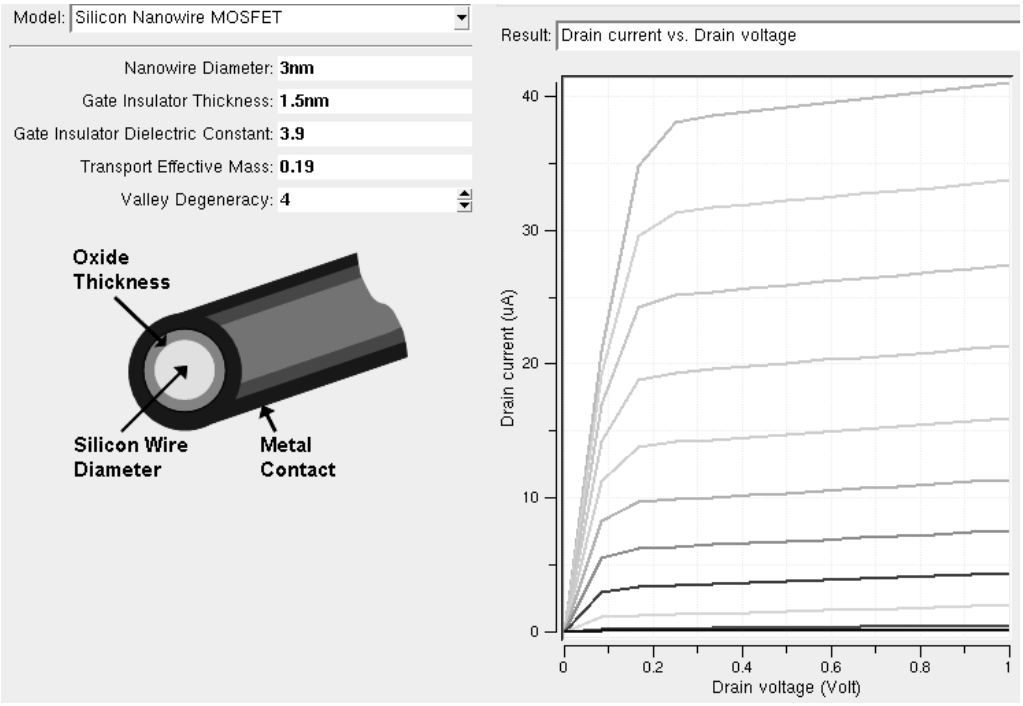

Fig. 3b: log I_DVs V_{DS} for k =3.9

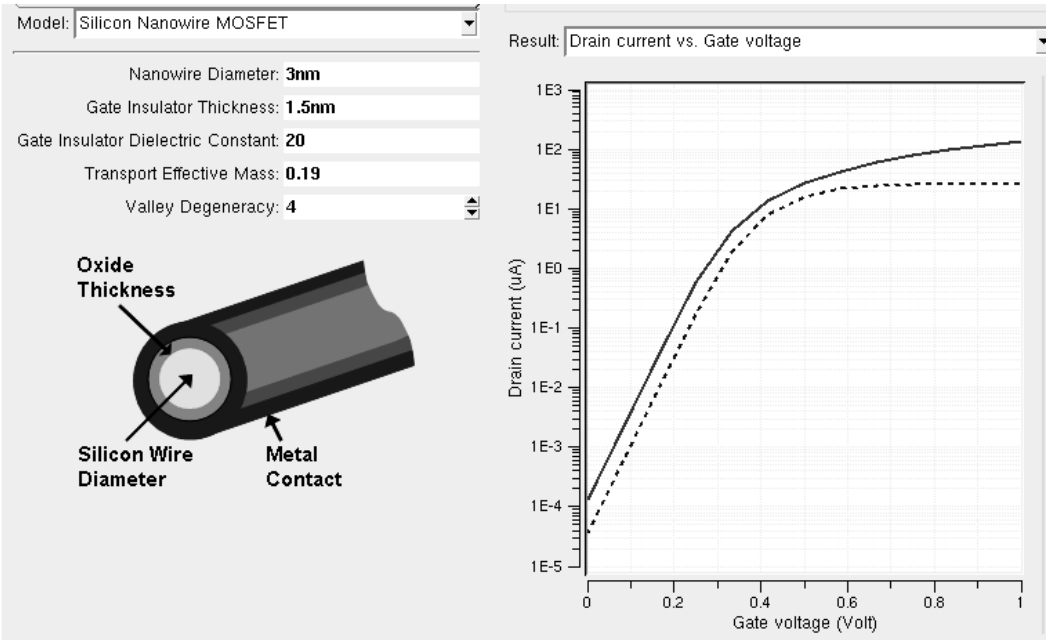

Fig 4a: log I_DVs V_{GS} for k = 20

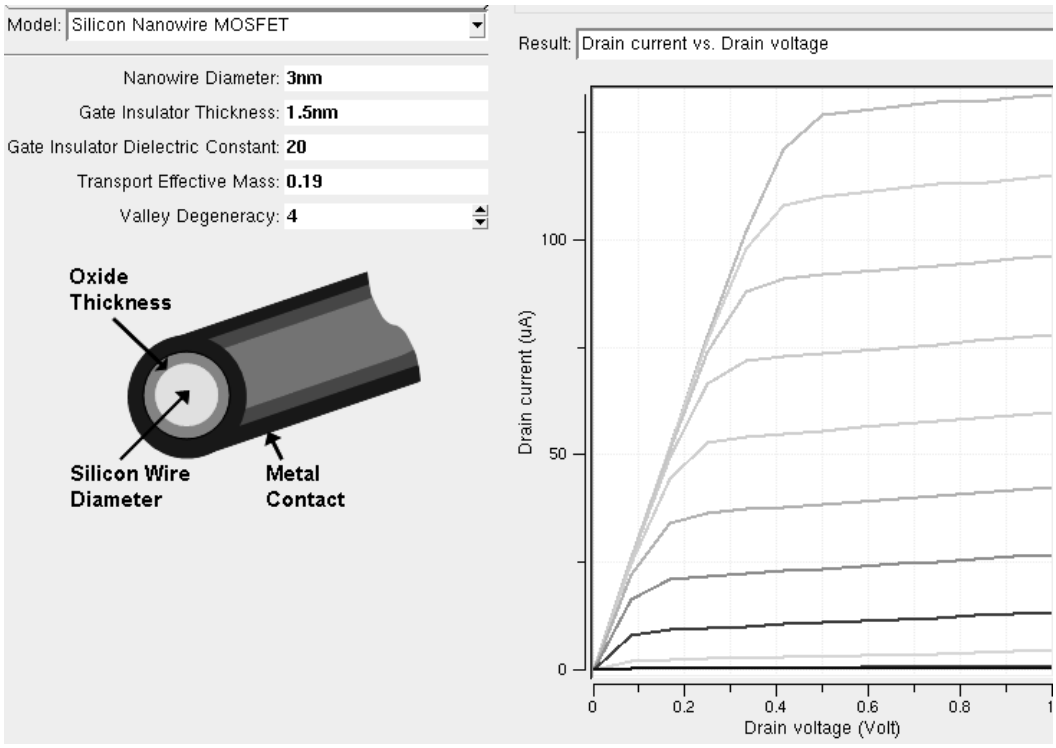

Fig. 4b: log I_DVs V_{DS} for k = 20

To explain this, we first need to obtain an expression for the nanowire FET current under low drain bias. From equation (9) under low brain bias (U_D<<1 or U_D<<$|\eta_F|$), therefore:

$$I = M\frac{qK_BT}{\pi\hbar}\frac{\partial\vartheta_0(\eta_F)}{\partial\eta_F}U_D = M\frac{qK_BT}{\pi\hbar}\frac{^{V_{DS}}/_{K_BT/q}}{1+e^{-\eta_F}}$$
$$= M\frac{2q^2}{\hbar}\frac{V_{DS}}{1+e^{-\eta_F}} \qquad (11)$$

The channel conduction of a nanowire FET is obtained as:

$$g_d = M\frac{2q^2}{\hbar}\frac{1}{1+e^{-\eta_F}} \qquad (12)$$

At the non-degenerate condition η_F< 0 and $|\eta_F|$>>1, i.e. the source Fermi level is well below the top of the barrier. As the gate voltage increases η_F is raised and the channel conductance increases. But once the full degenerate condition (i.e. the source Fermi level is well above top of the barrier) is satisfied, the channel conductance saturation to a fixed value (independent of any device parameters).

$$g_d = M\frac{2q^2}{\hbar} \text{ (Full degenerate)} \qquad (13)$$

Which is called quantum conductance.

RESULT

For the SNWFET with a HFO2 layer (K=20), due to large gate capacitance, the top of the barrier can be efficiently lowered by increasing the gate voltage. Consequently , the device easily enters to the full degenerate regime when the gate bias is larger than 0.5V. For the SNWFET with a SiO_2 layer (K=3.9), however, the gate capacitance is significantly lower than that for K=20 and the full degenerate condition cannot be achieved at the bias range (0V-1V) , which is used in this simulation.

CONCLUSION

In this paper, we presented a simple, analytical theory of ballistic nanowire FETs, The mode was derived by modifying an analytical approach that was previously used for ballistic planer MOSFET. A coaxial SNWFET was simulated using this model and the results illustrate the essential physics and peculiarities of 1D nanowire FETs , such as saturation of channel conductance at the full – degenerate limit and the saturation transconductanceat the quantum capacitance limit and full degenerate limit.

REFERENCE

1. Z. Ren, "Nano scale MOSFET: Physics, simulation and Design," Ph.D. Thesis, Purdue University, 2001
2. J.wang and M Lundstrom, "Ballistic Transport in high electron mobility transistors" IEEE Trans. Electron. Devices, vol 50, no 7, pp 1604-1609, Jul.2003
3. P.M. Solomon and S.E.Laux, "The ballistic FET:design, capacitance and Speed limit," IEEE international Electron Dev. Meeting (IEDM) Tech, Digest pp 95-98 2001
4. P. Natori , A Rahman, J Guo, "Theory of ballistic nano transistor" IEEE Trans. Electron Dev., vol 50,no 9,pp1853-1864, sep2003
5. H.Wongekal, "Device design considerations for double gate , ground plane, and single gate ultrathin SOI MOSFET at the 25nm channel length generation", IEEE Int. Electronic Device Meeting (IEDM) Tech. Digest pp 407-410, Dec 1998.

6. H. Majima, Y. Saito, and T. Hiramoto, "Impact of quantum mechanical effects on design of nano scale narrow channel n- and p- type MOSFETs", IEEE Int. Electronic Device Meeting (IEDM) Tech. Digest pp 951-954, Dec 2001.
7. S. M. Sze, "Physics of semiconductor devices", 2nd edition, New York, Wiley 2015.
8. K. Kim, K.K. Das, R.V. Joshi, " Leakage power analysis of 25nm double gate CMOS devices and circuits", IEEE transaction on Electronic Devices, Vol 52, no 5, pp 980-986, 2005.
9. Z.H. Liu et.al. "Threshold voltage model for deep-sub micrometer MOSFET", IEEE Transaction on Electronic devices, vol 40, no. 1, pp 86-95, 1993.